

FIG. 1

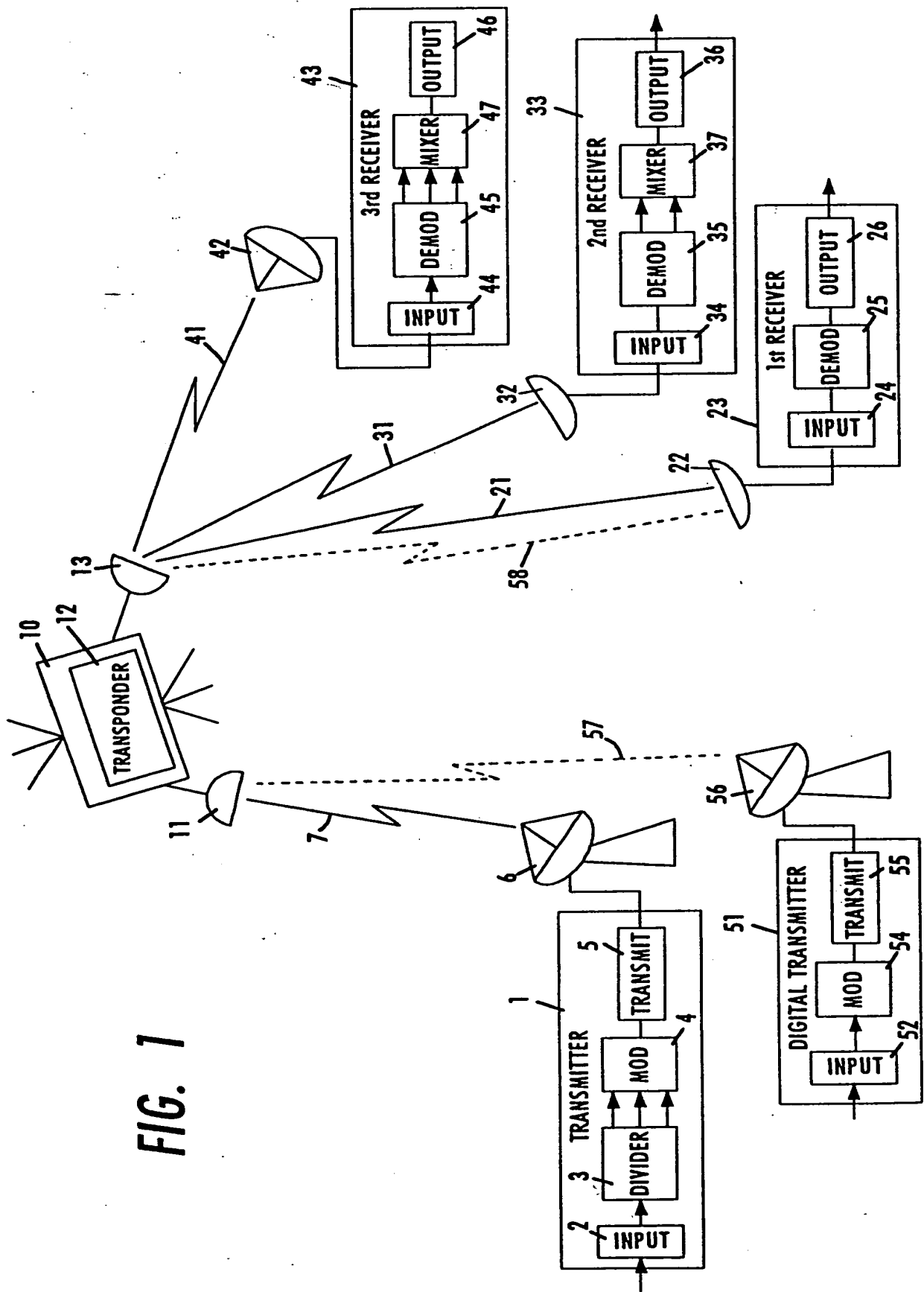
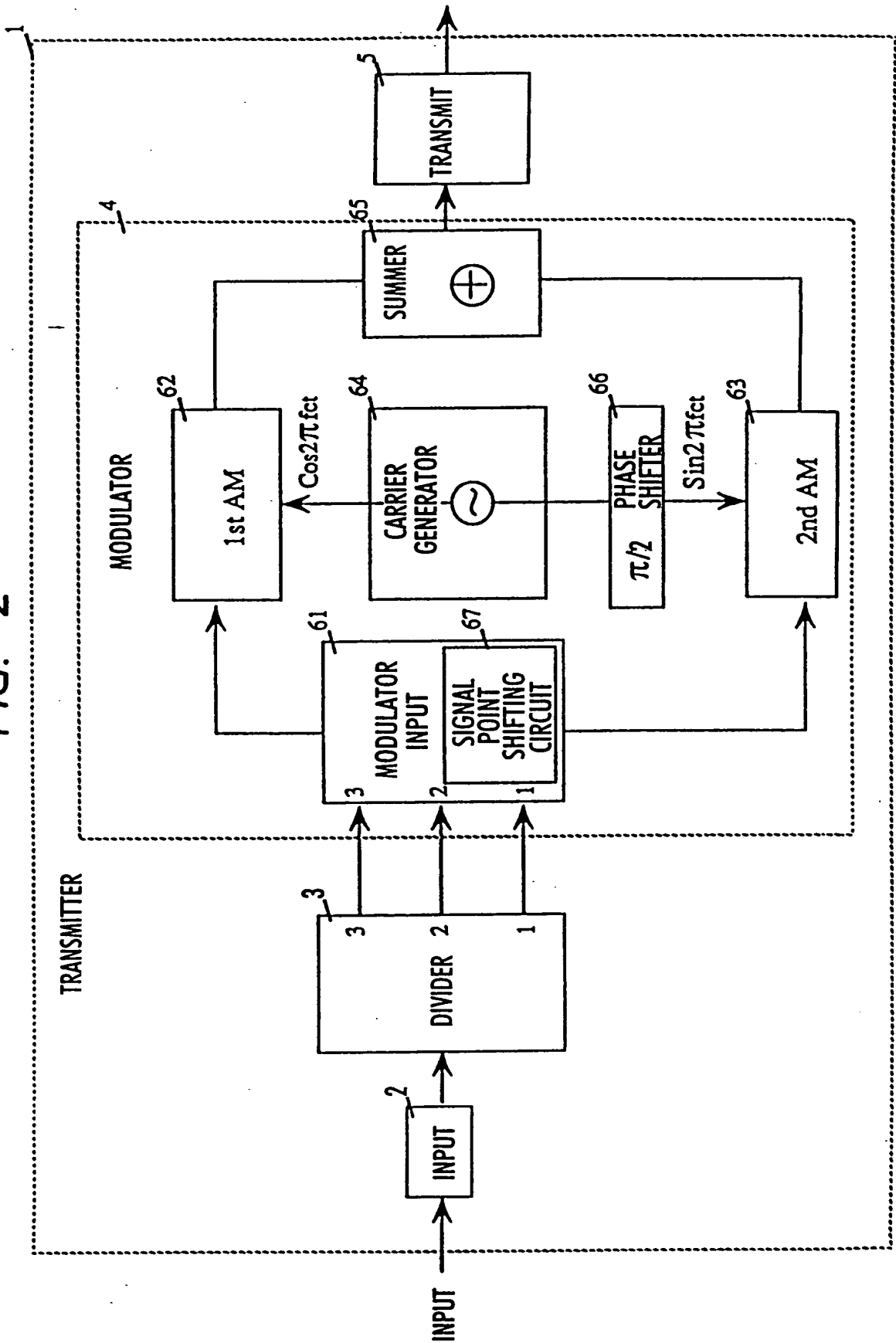
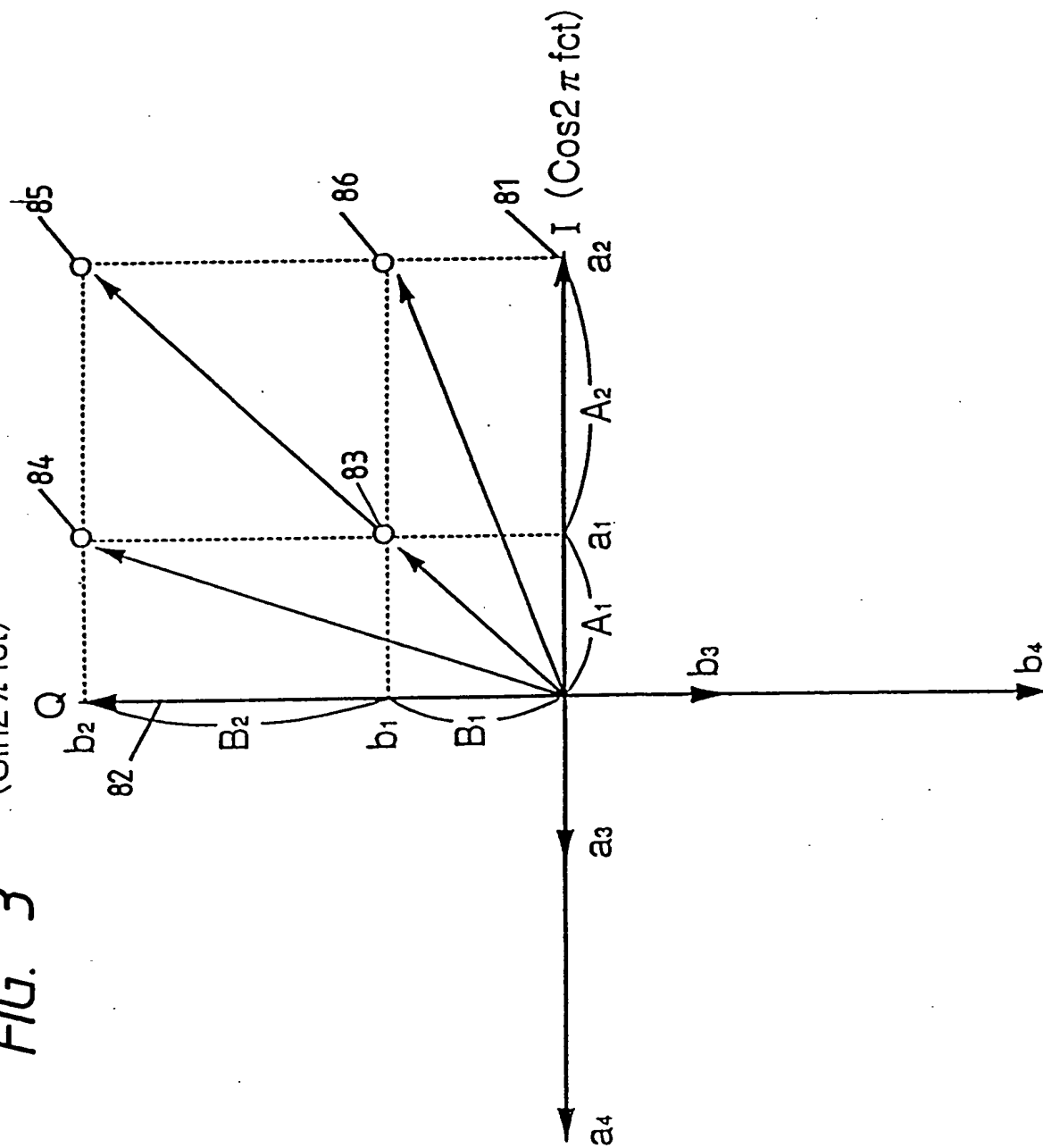


FIG. 2



( $\sin 2\pi \text{ fct}$ )

FIG. 3



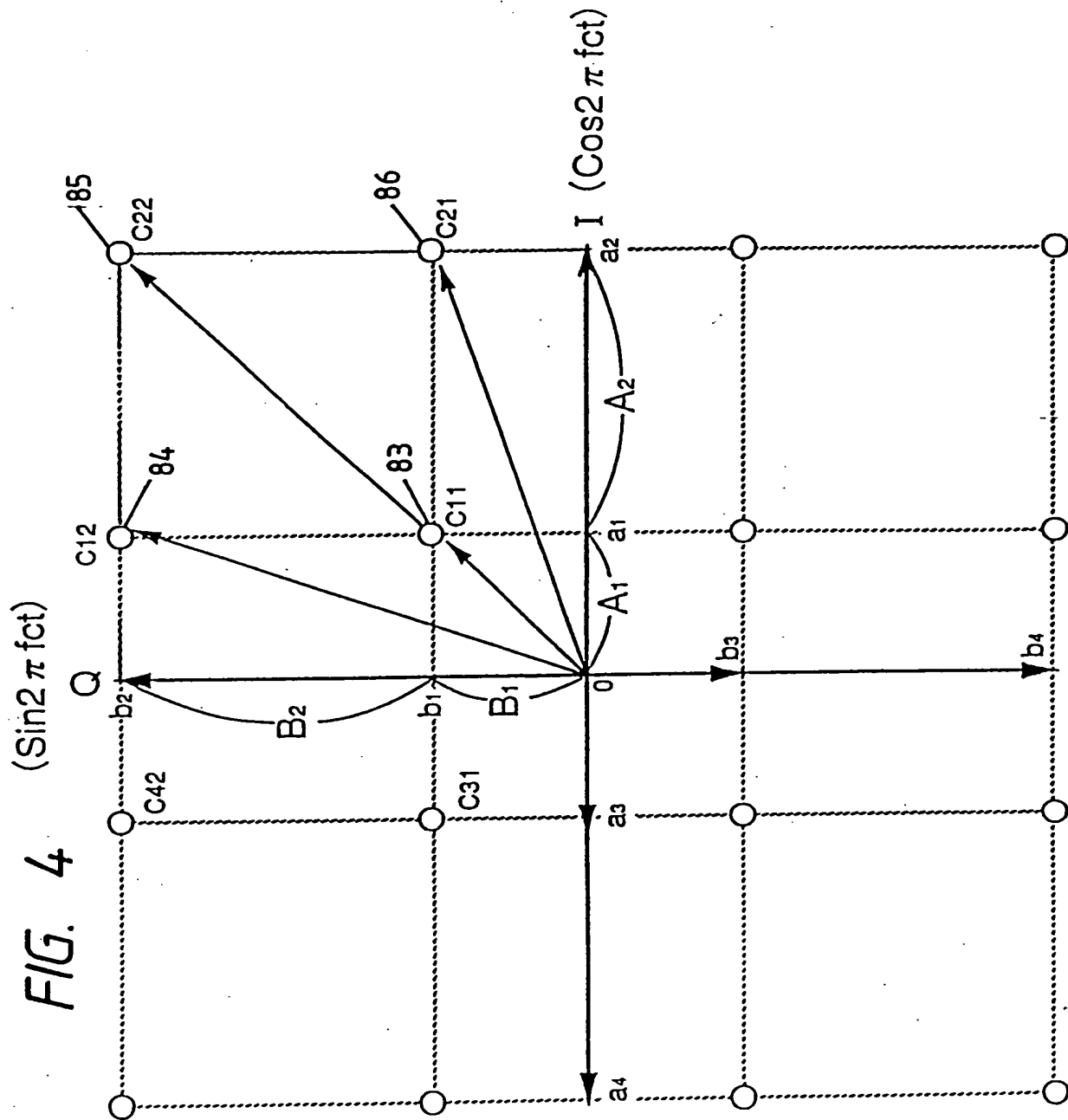


FIG. 5 ( $\sin 2\pi \text{ fct}$ )

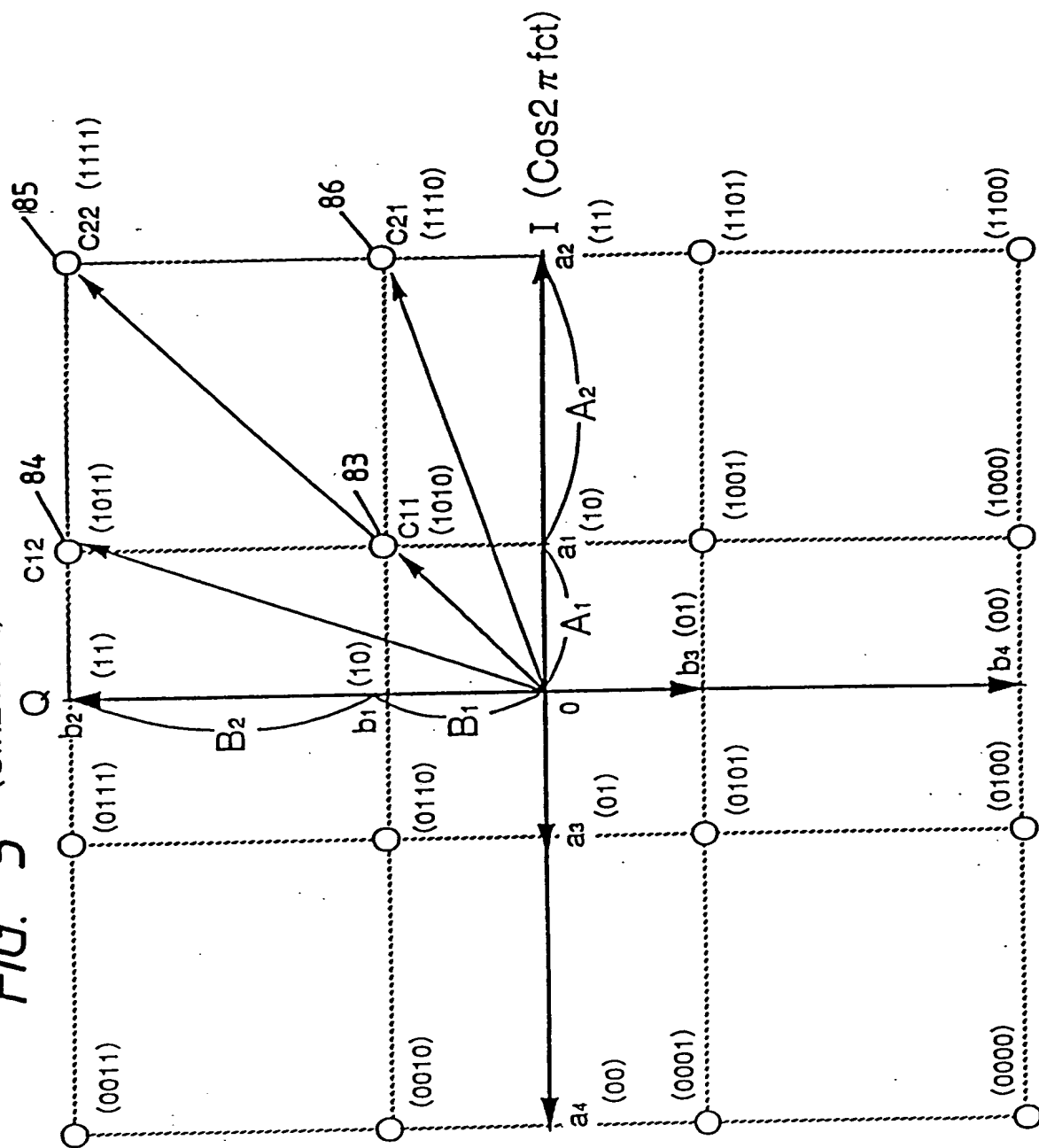


FIG. 6

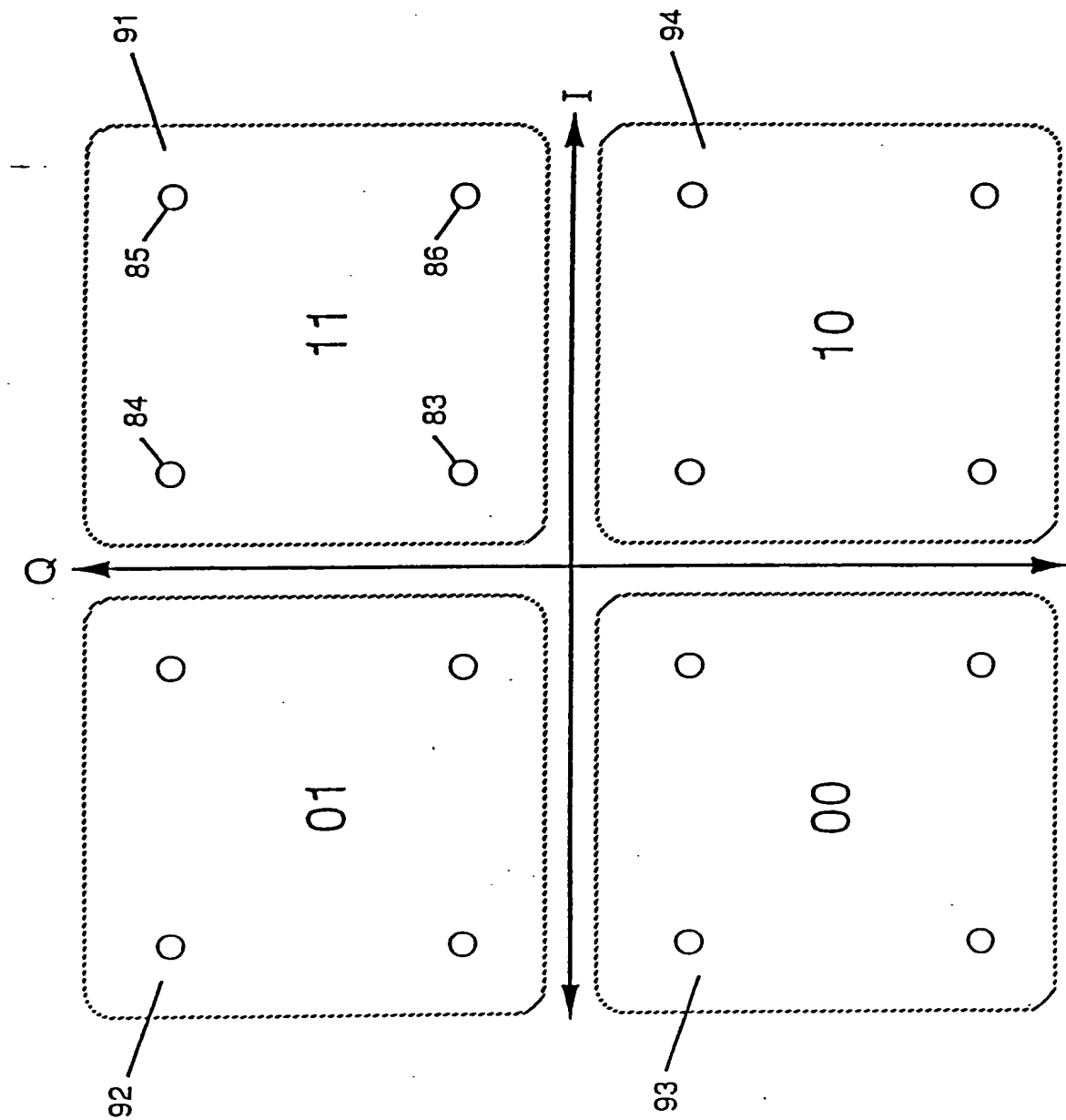


FIG. 7

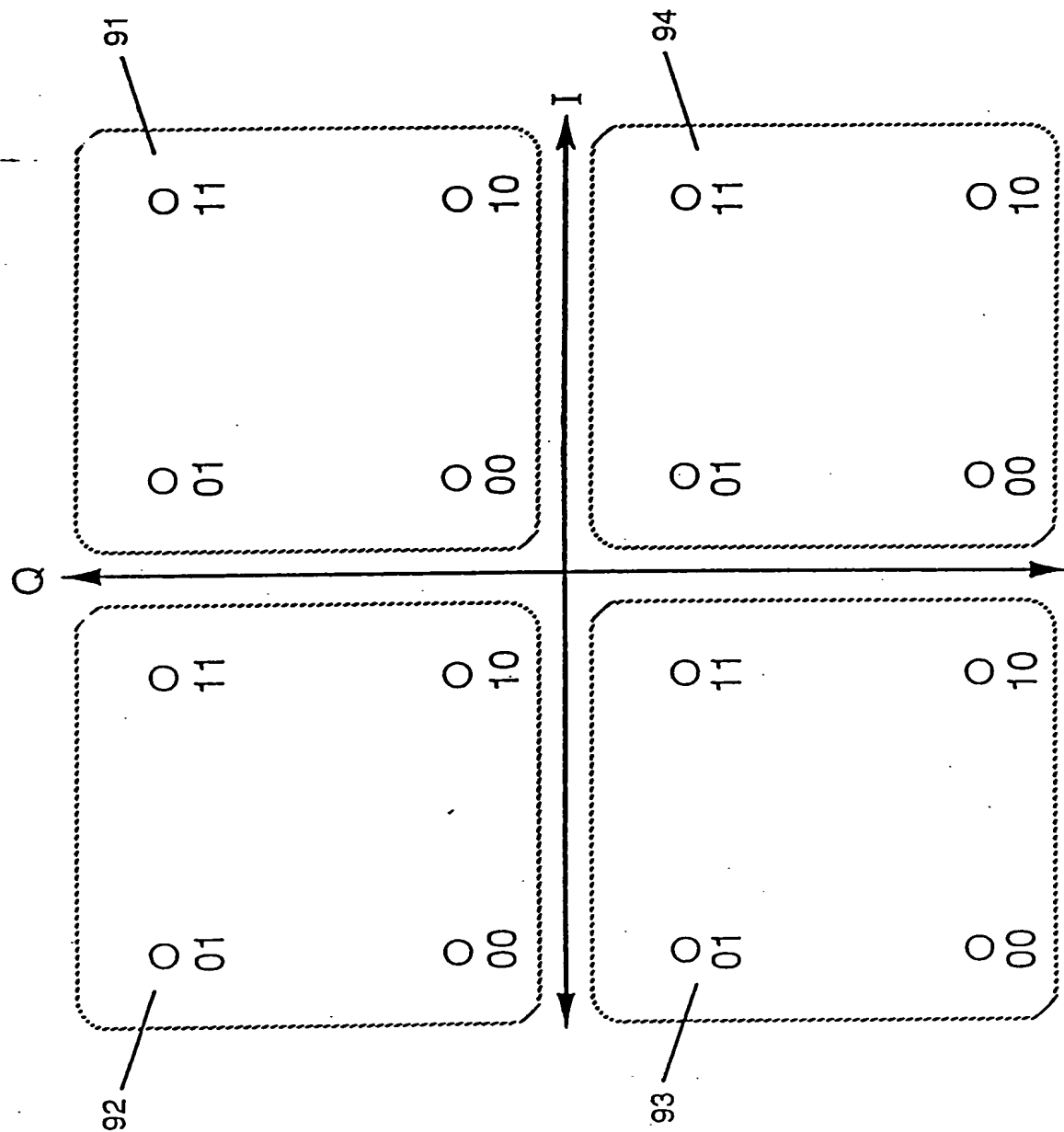


FIG. 8

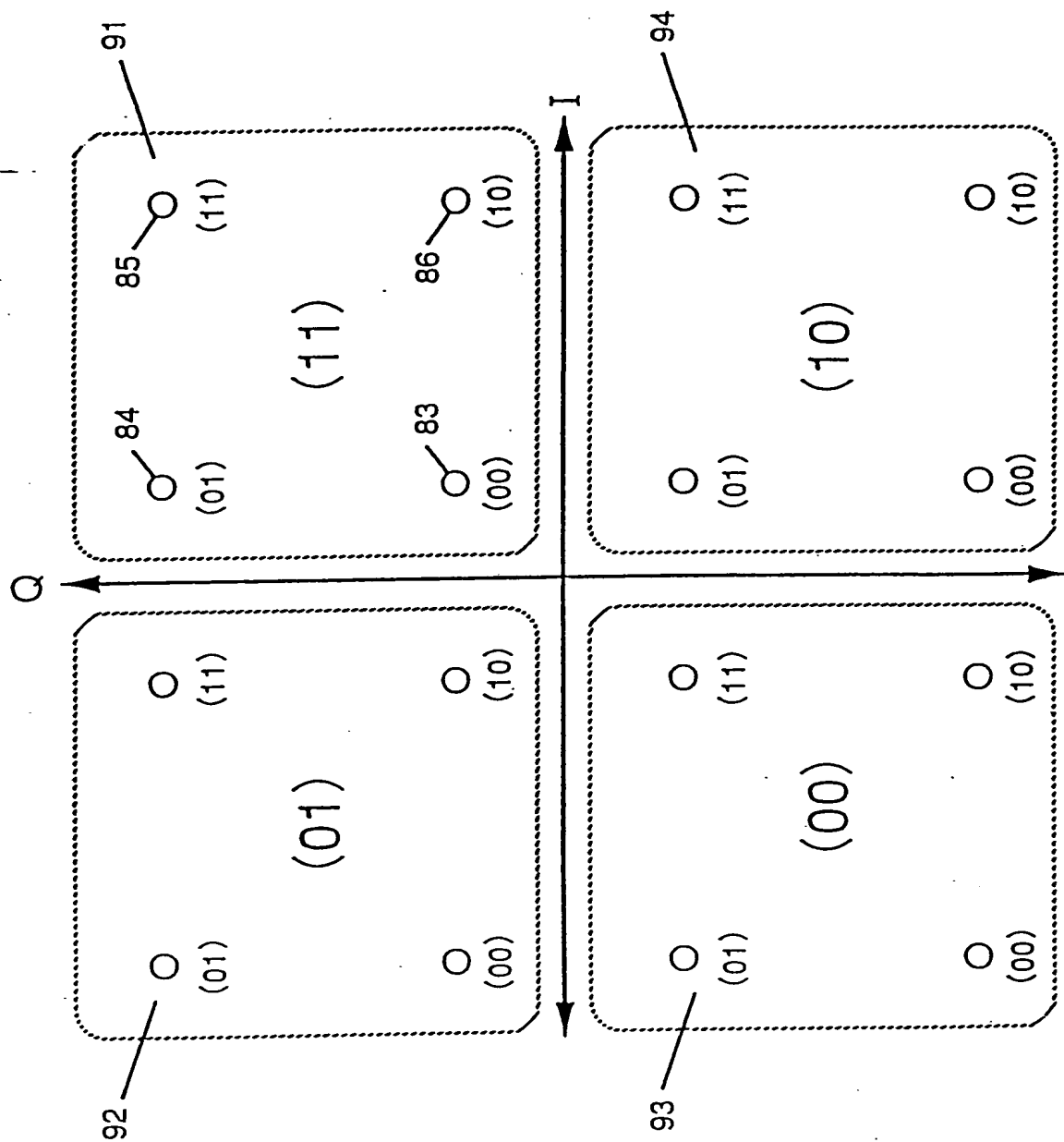




FIG. 9

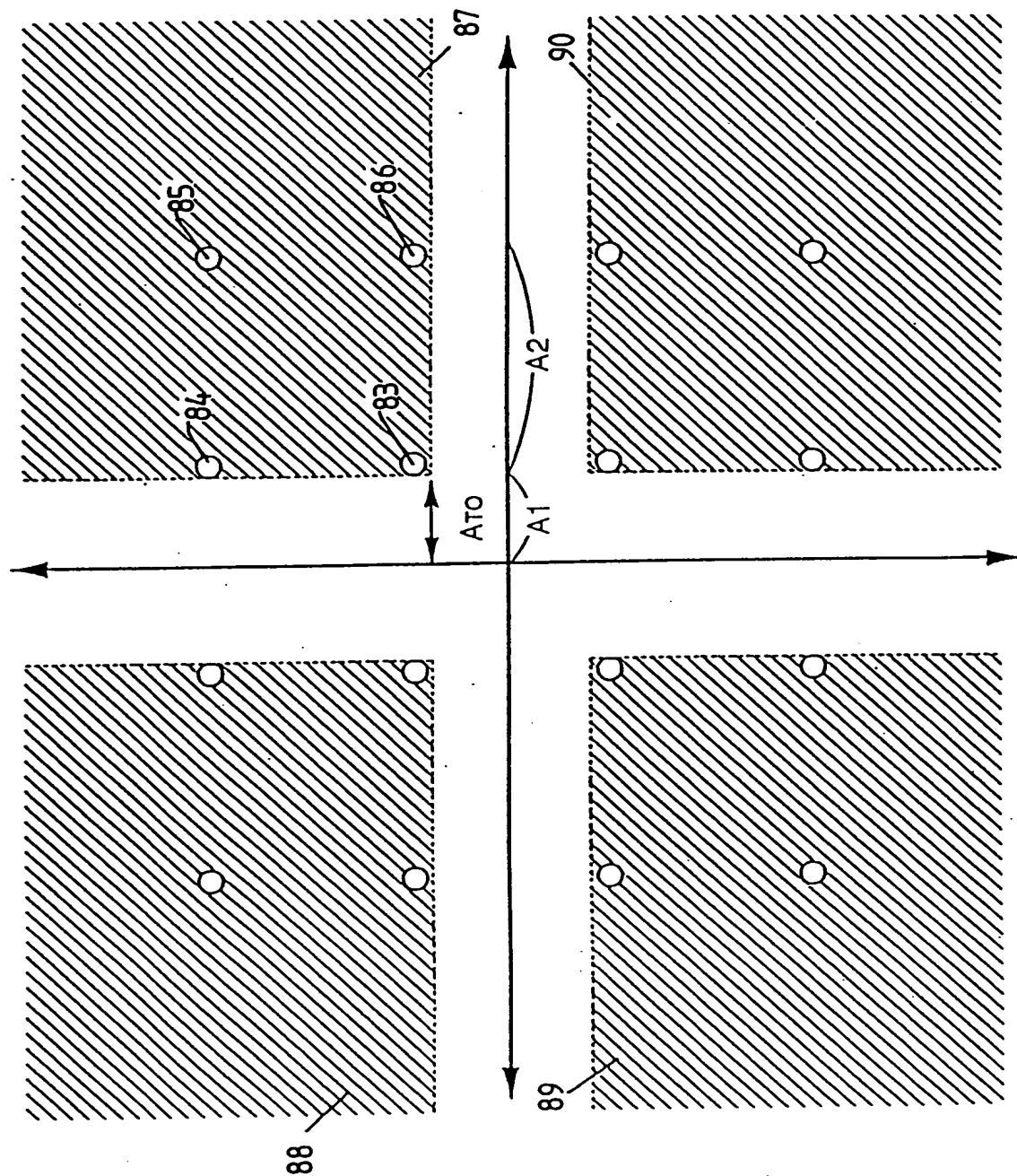


FIG. 10

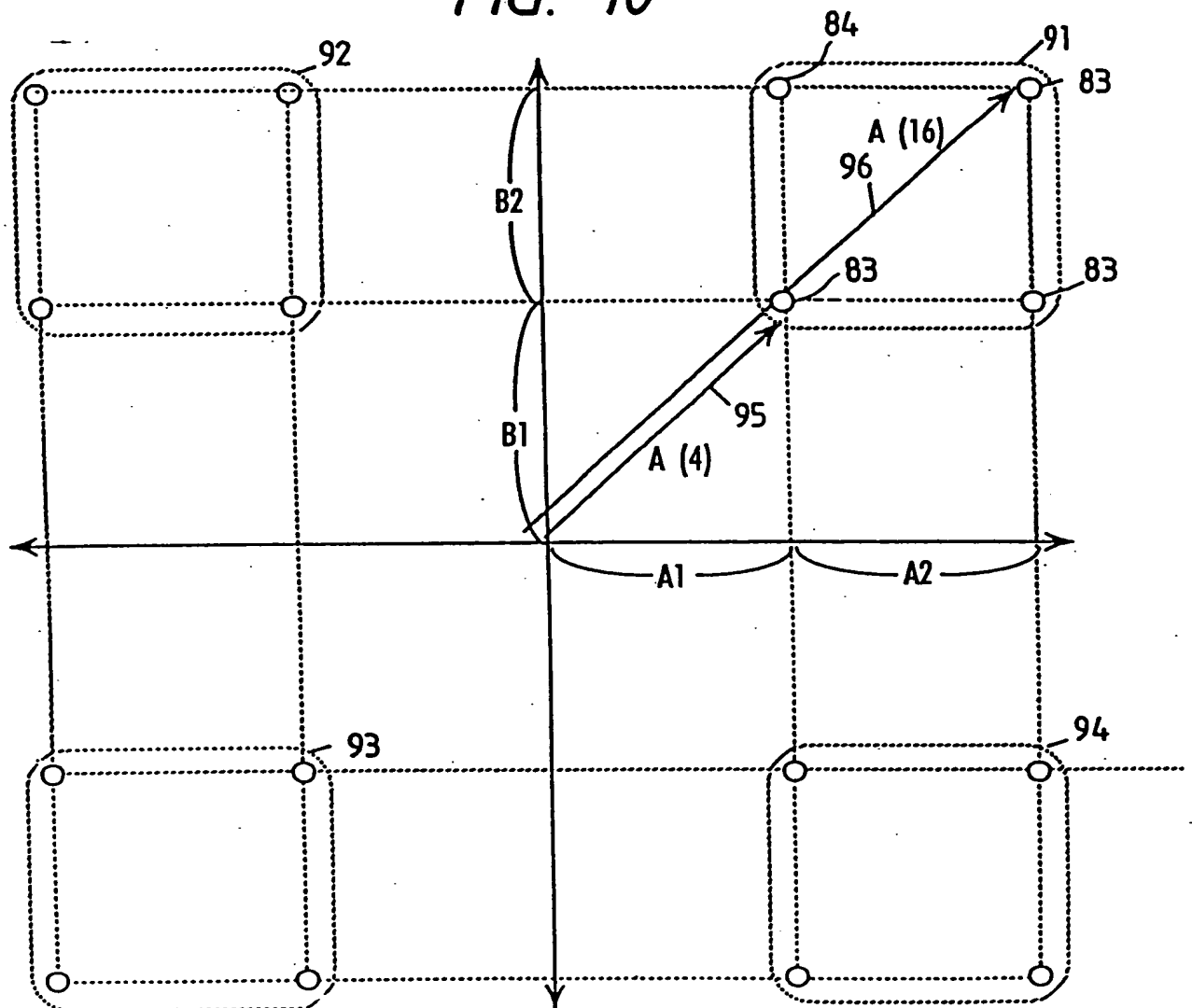


FIG. 11

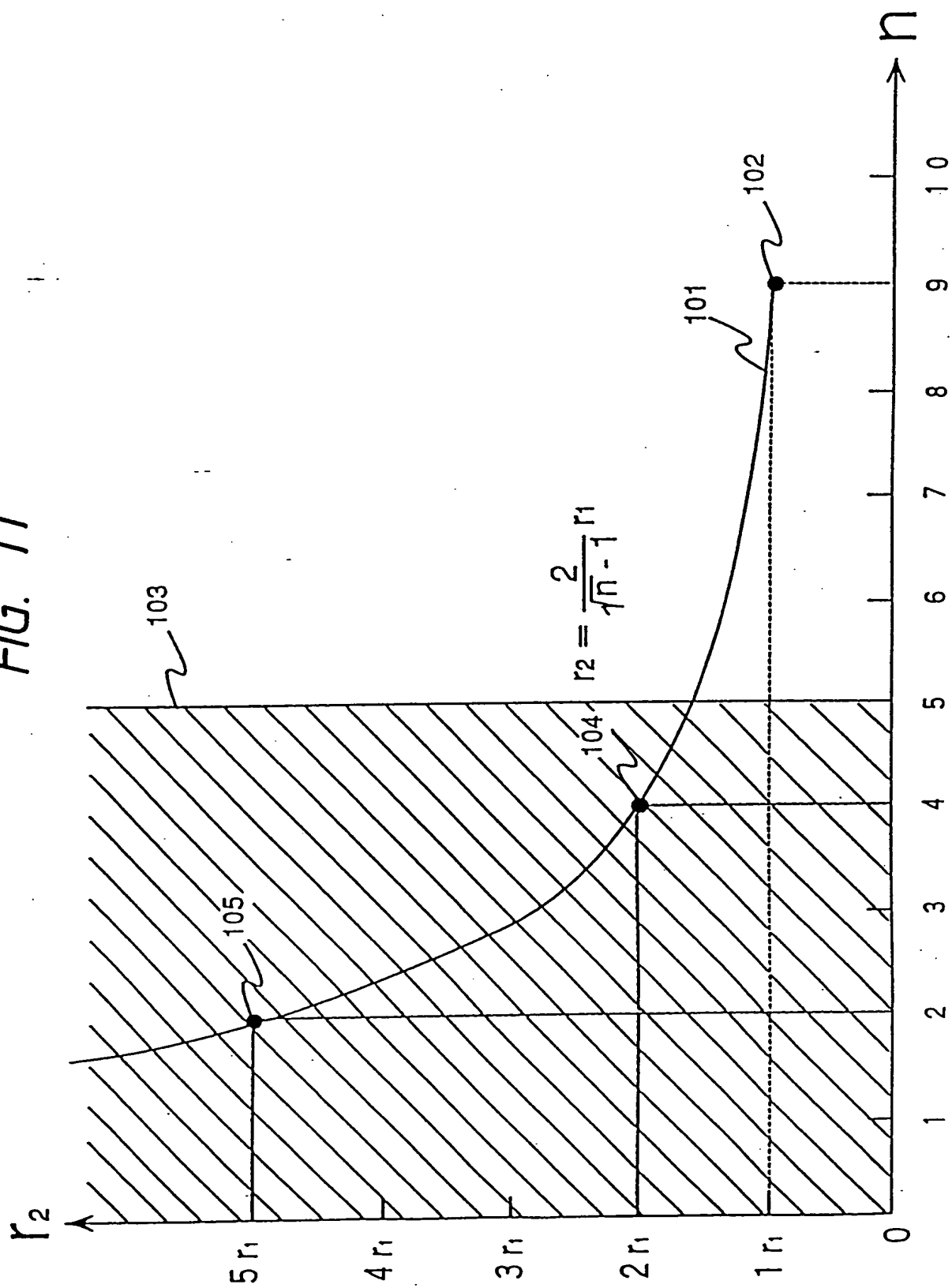


FIG. 12

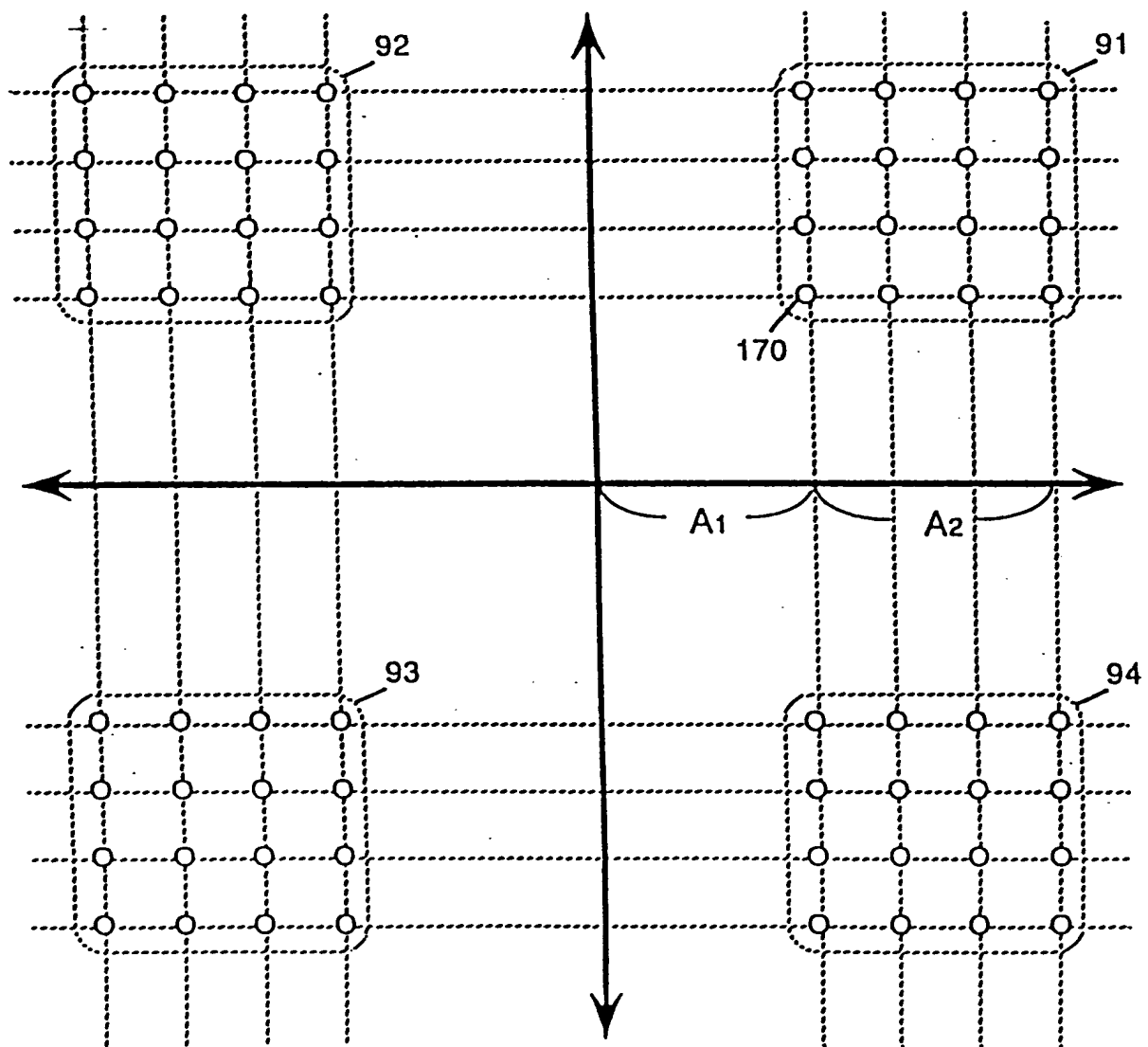


FIG. 13

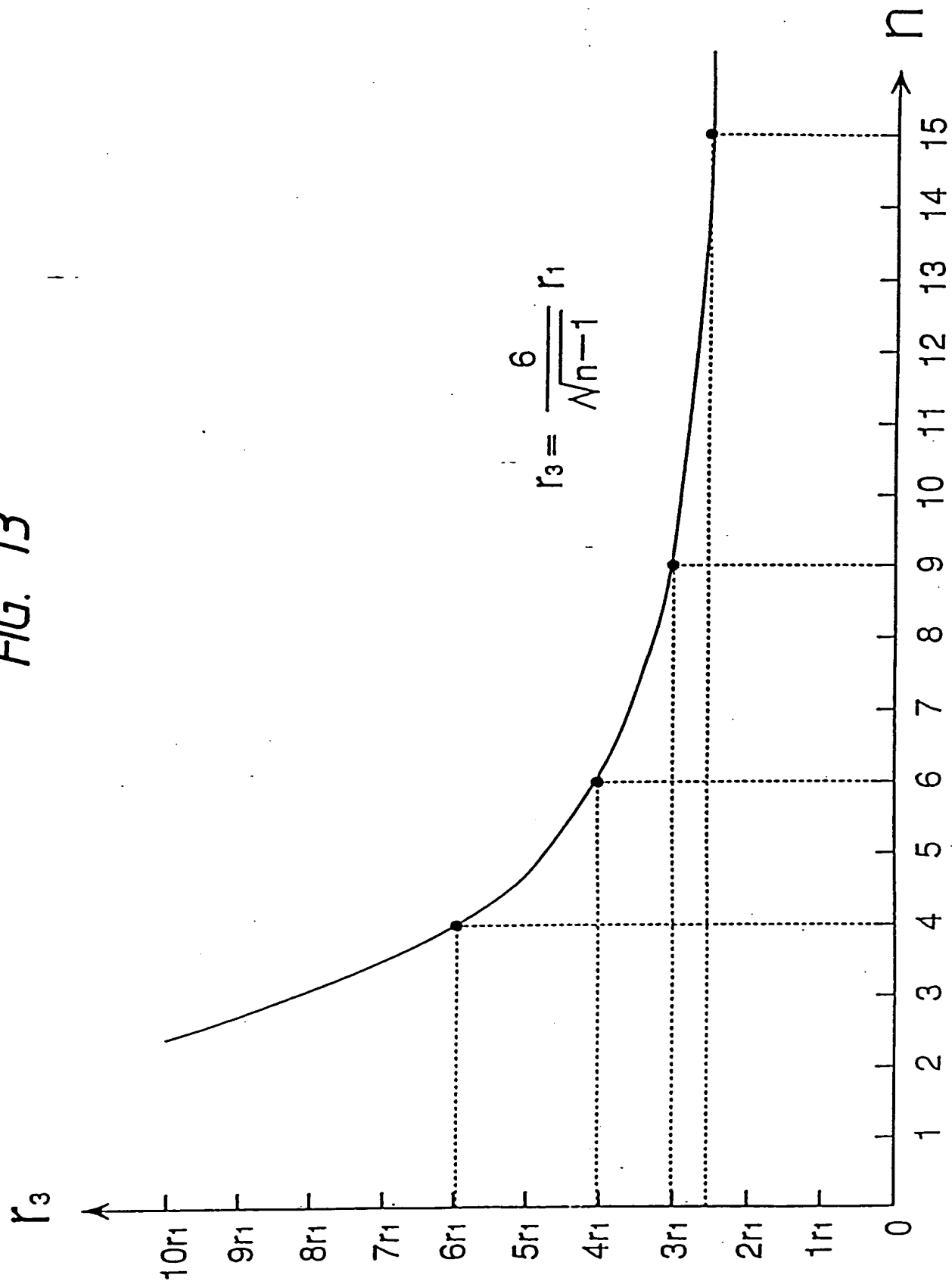


FIG. 14

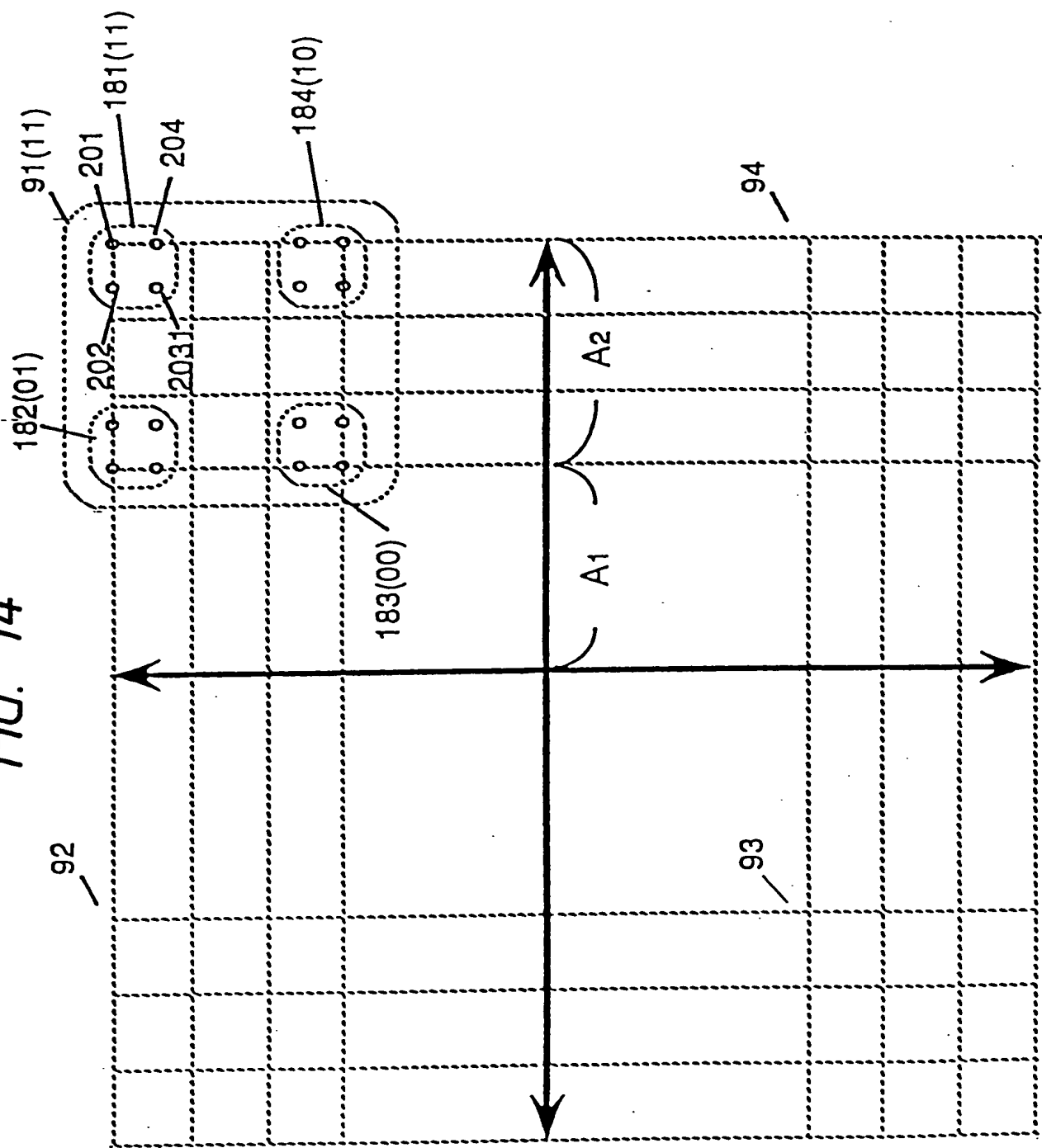


FIG. 15

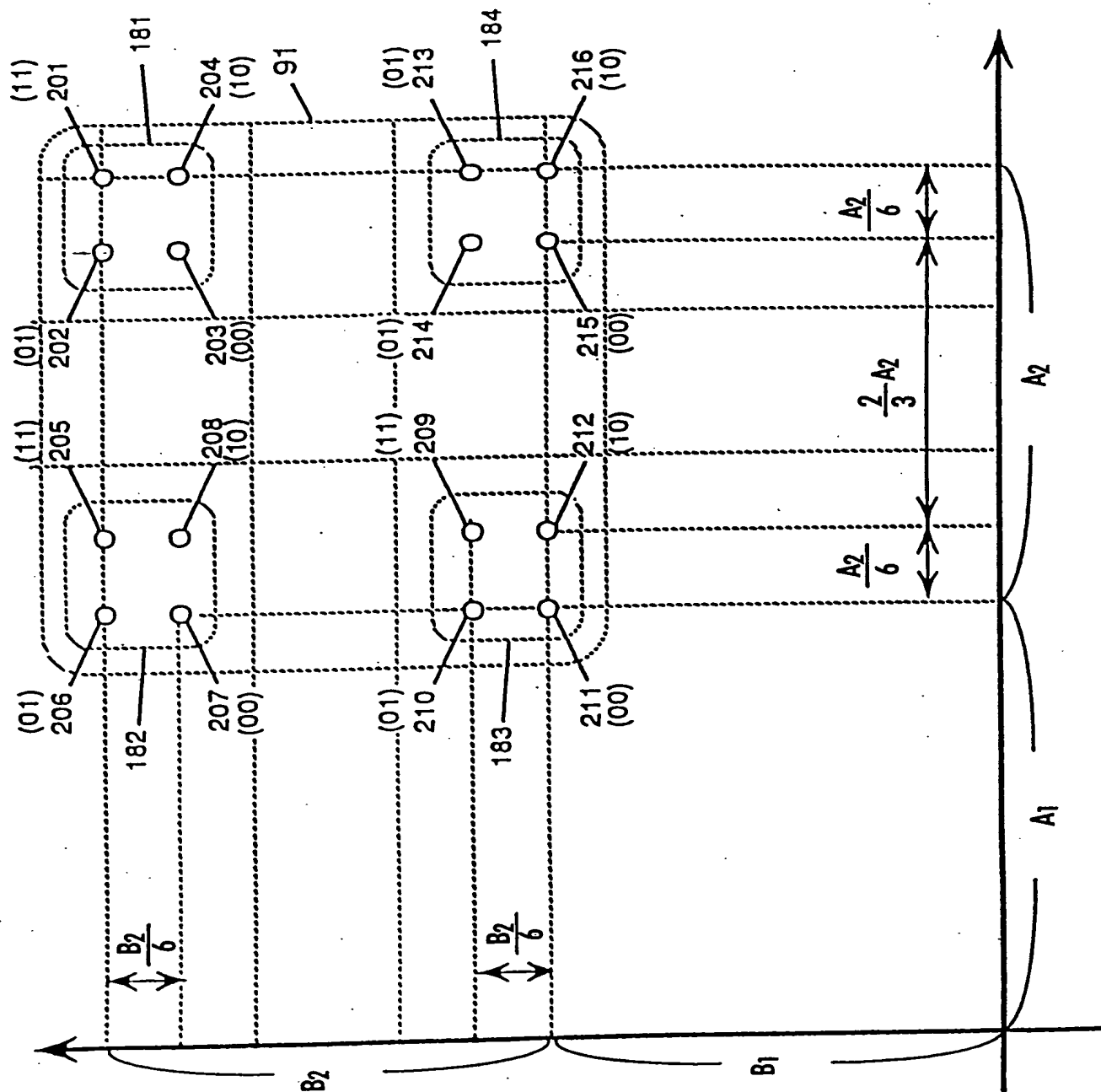
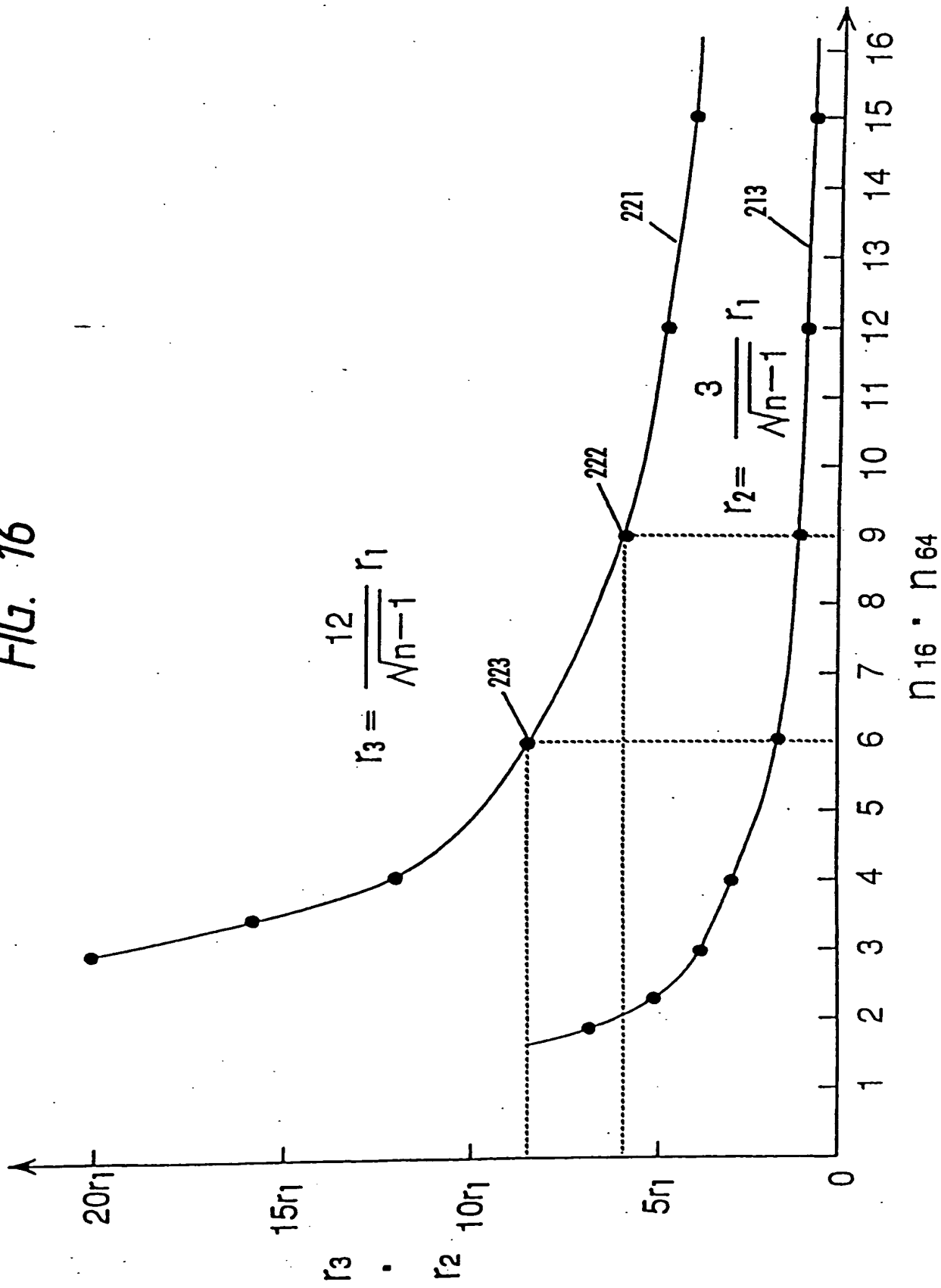


FIG. 16





**FIG. 17**

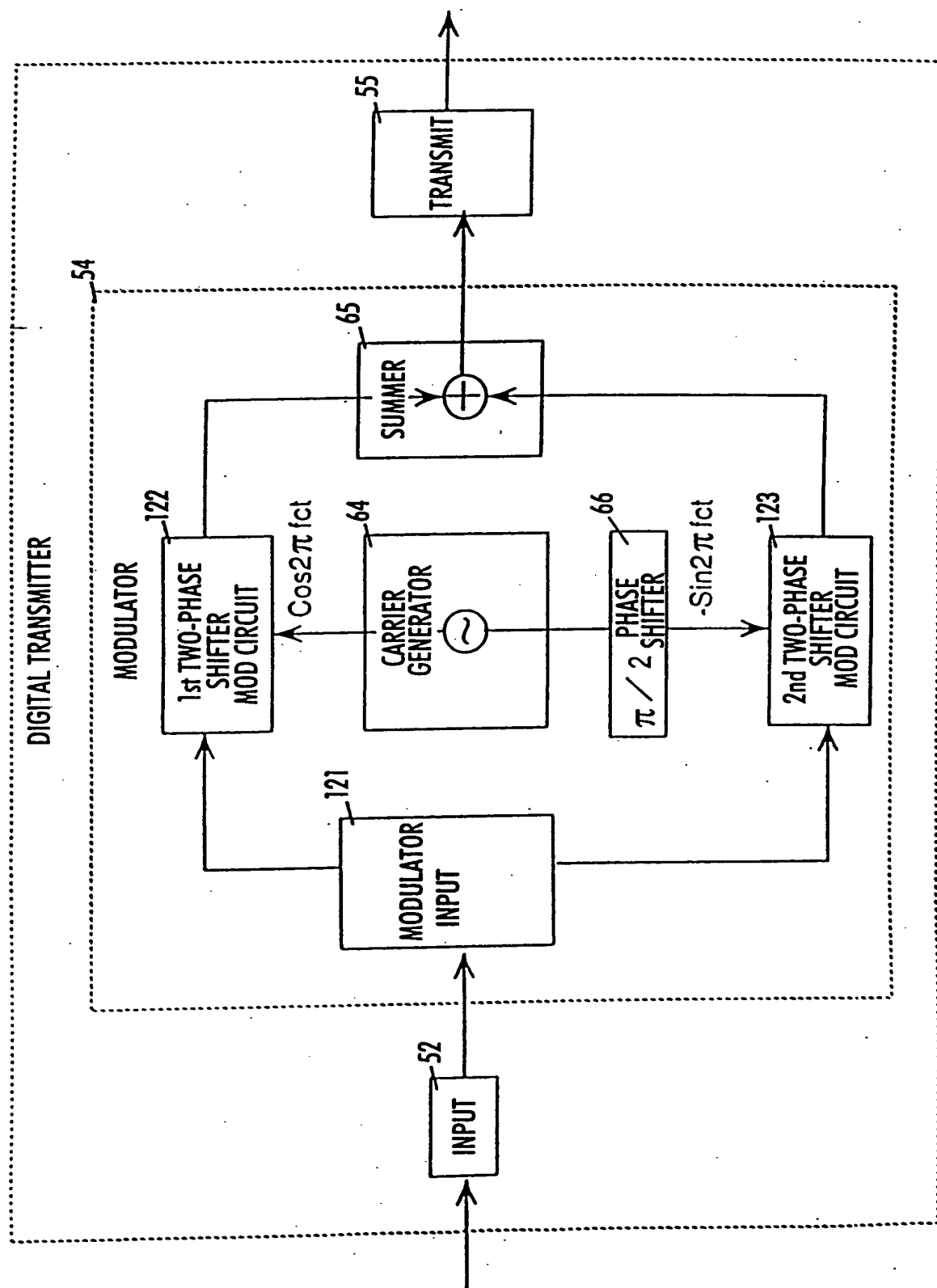


FIG. 18

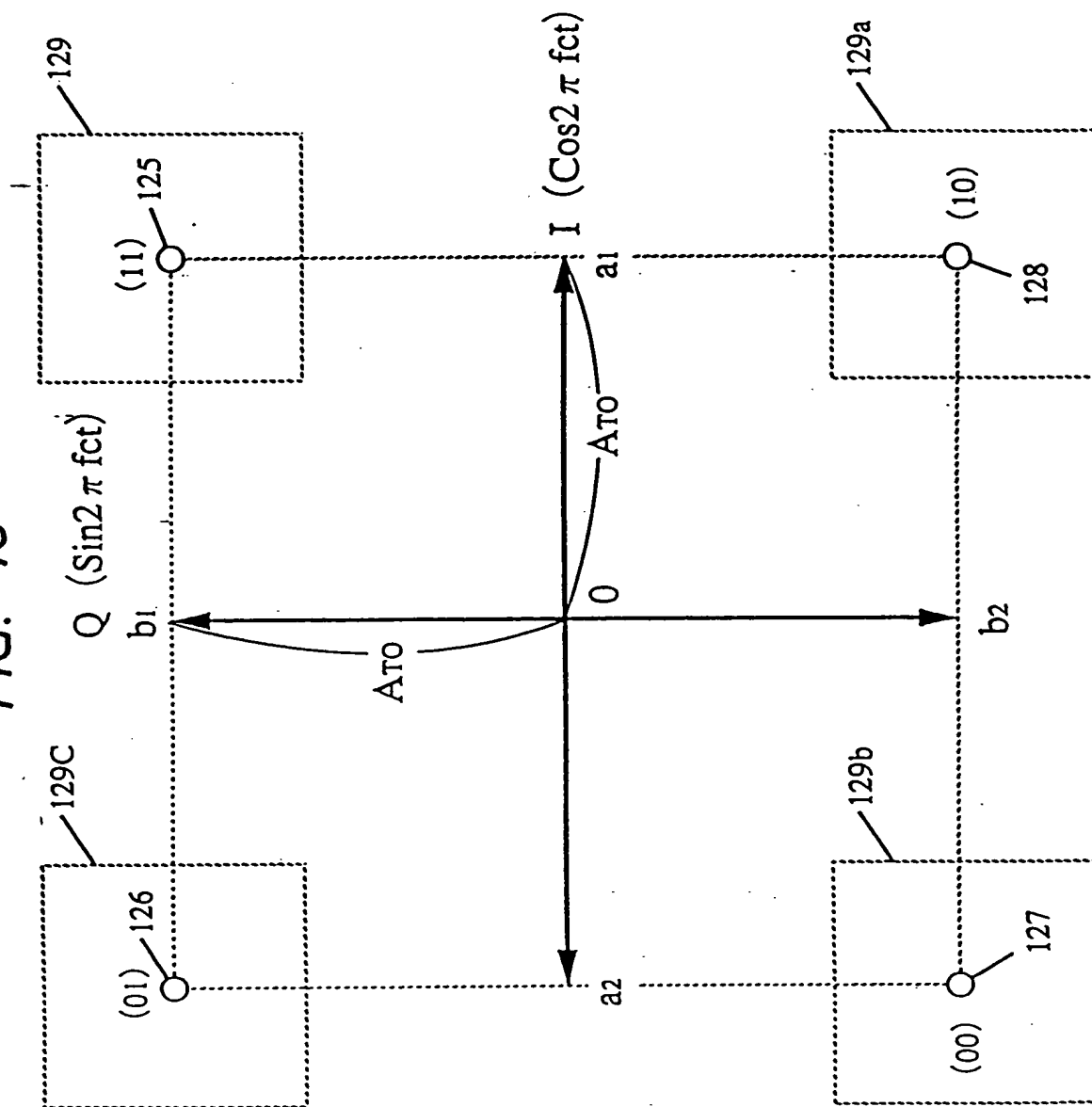


FIG. 19

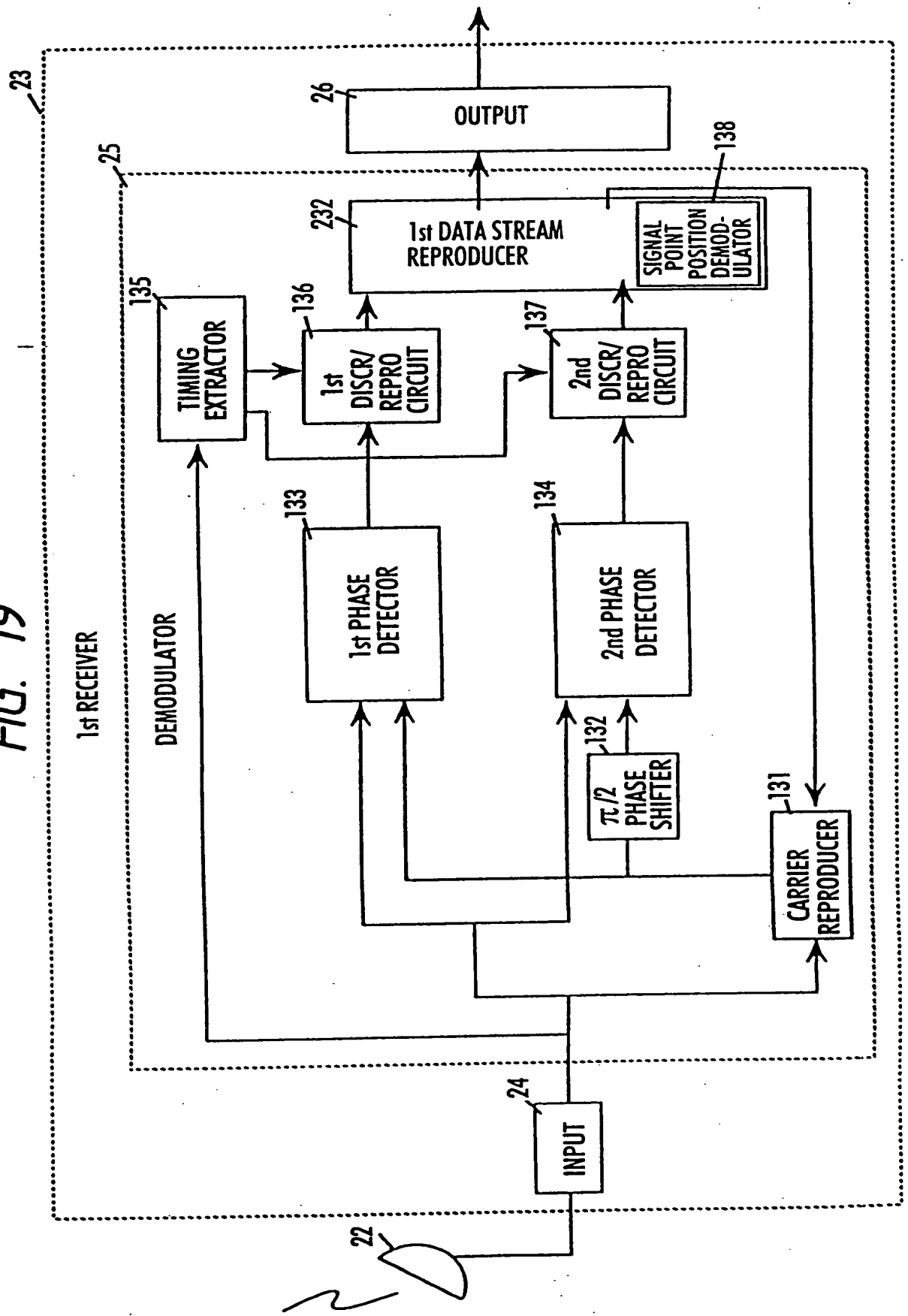


FIG. 20

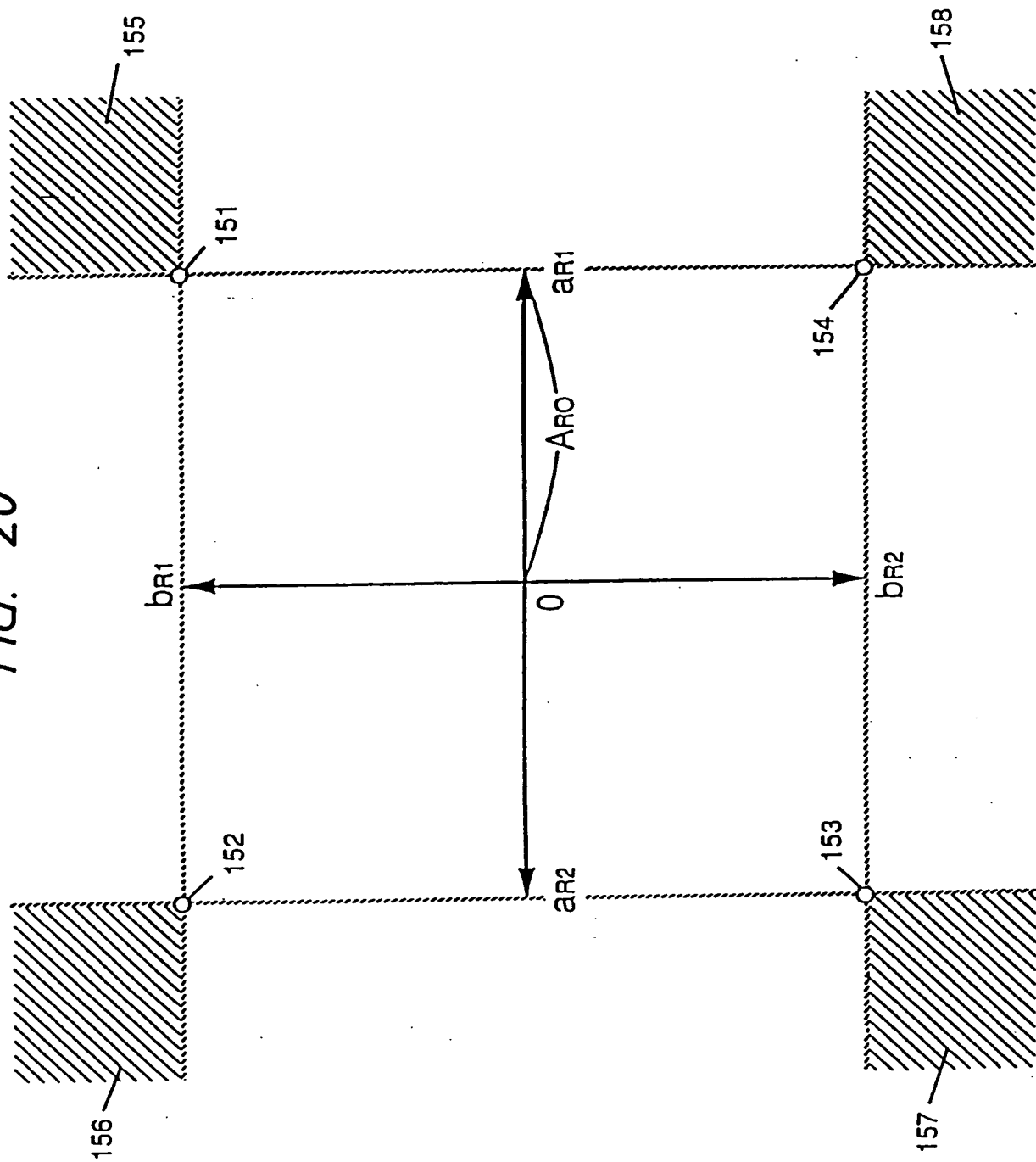


FIG. 21

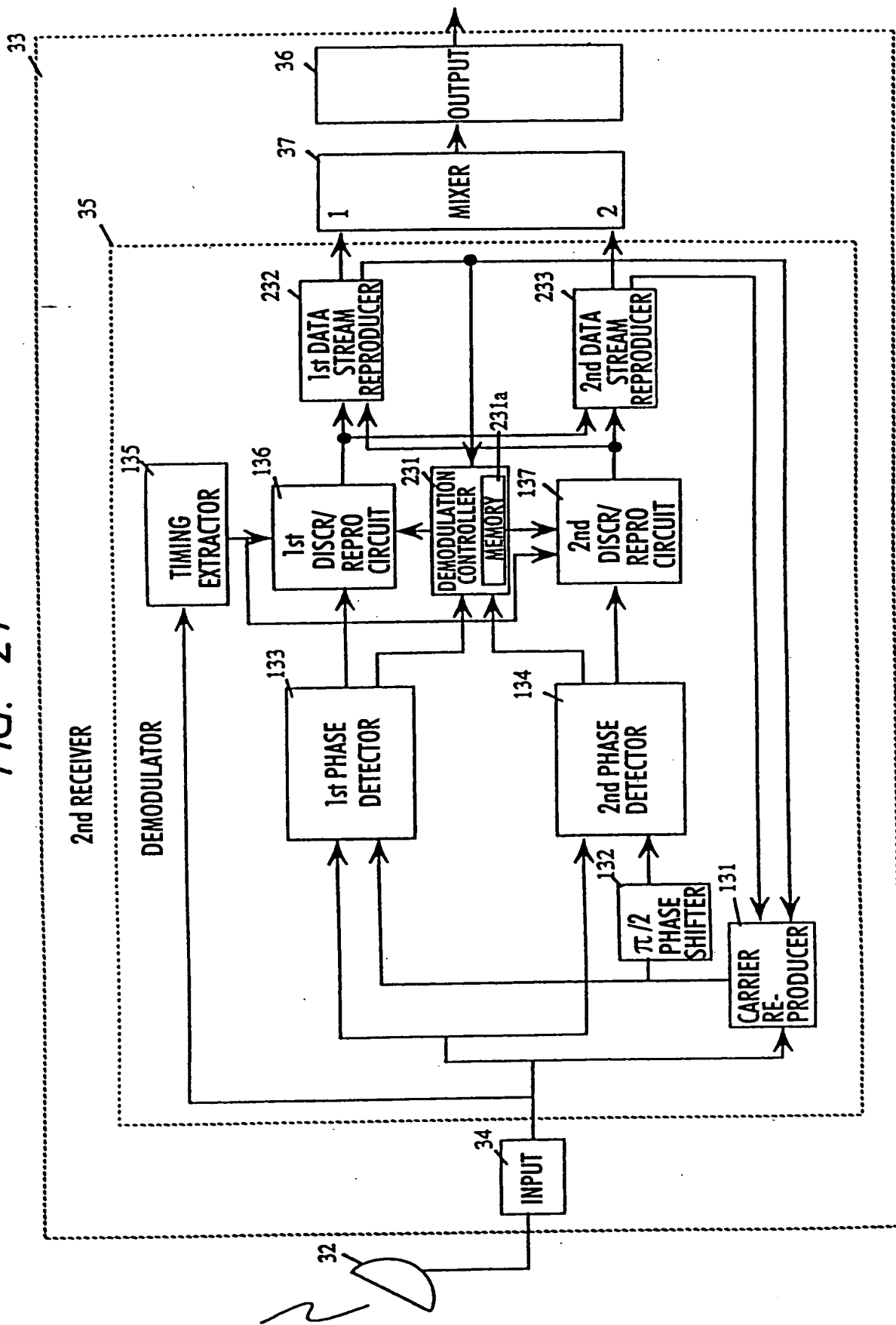


FIG. 22

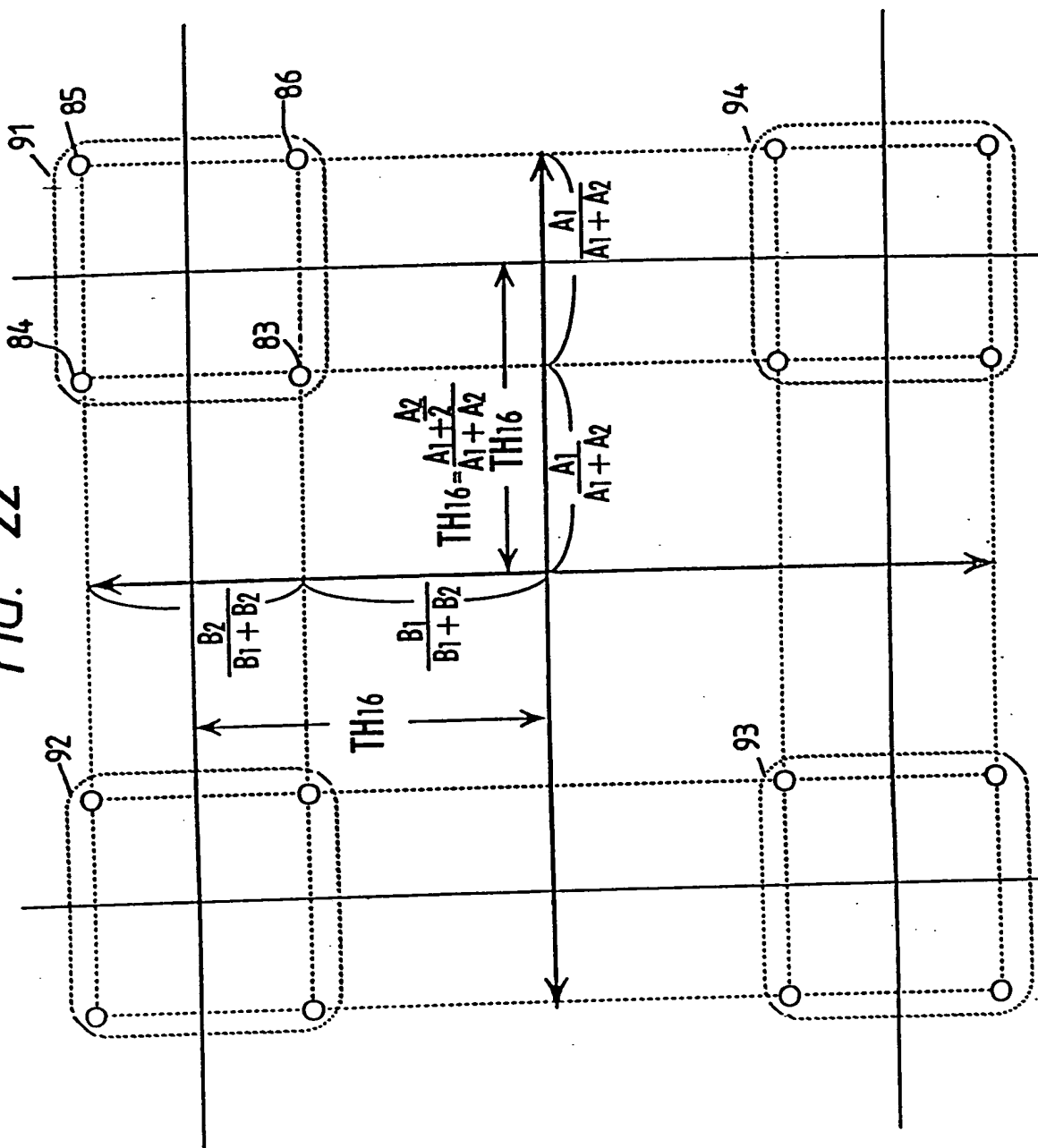
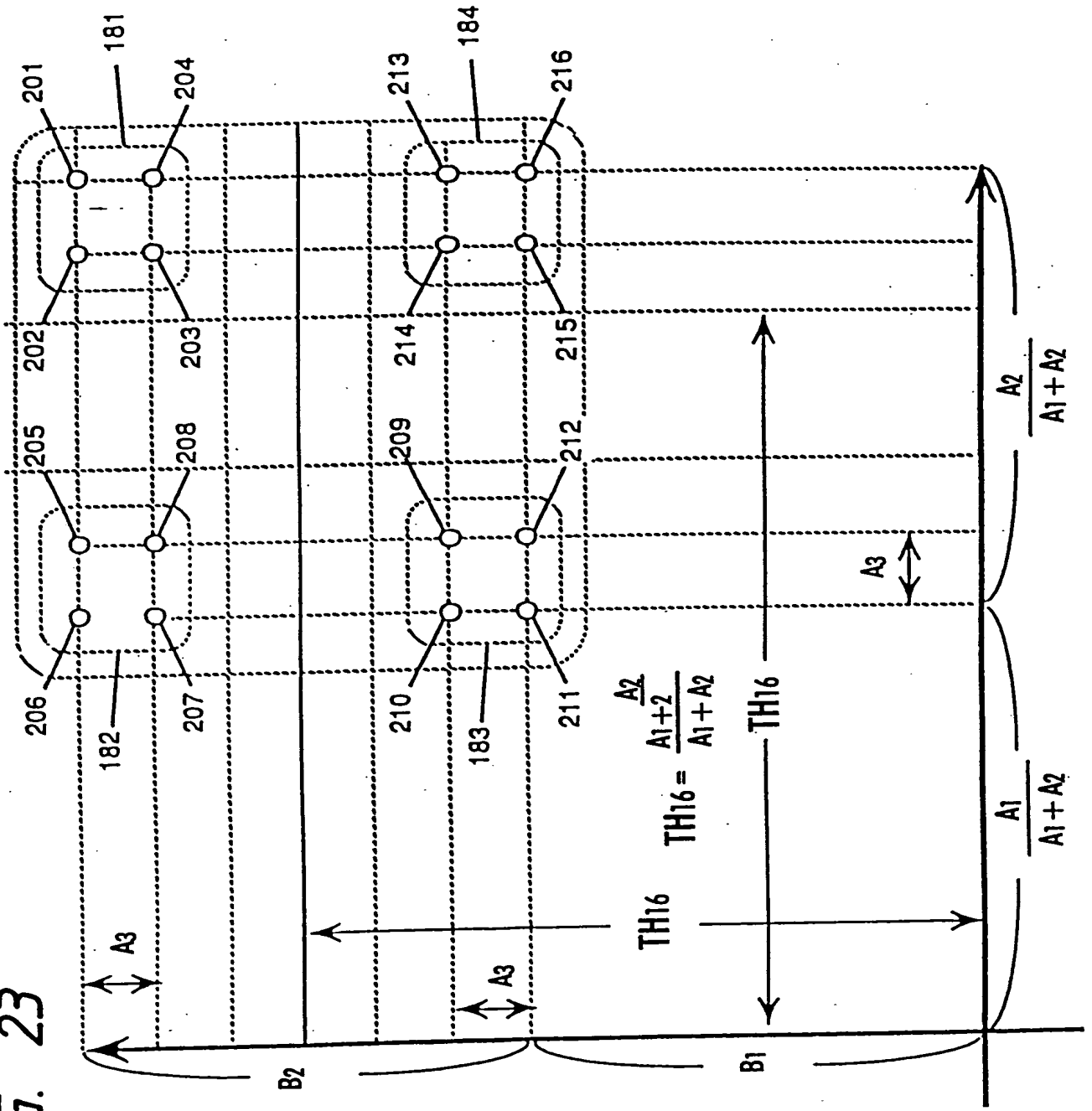
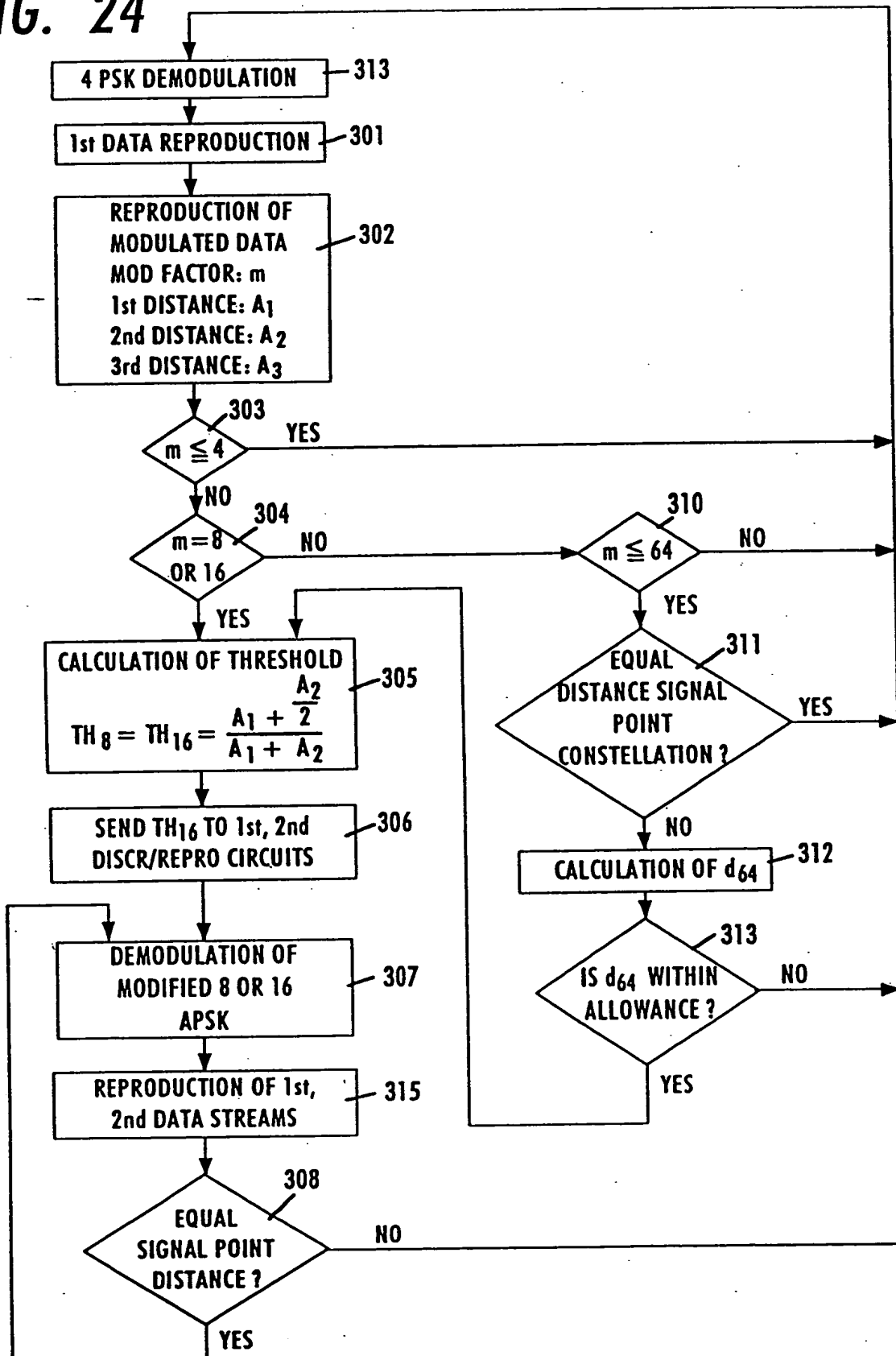


FIG. 23

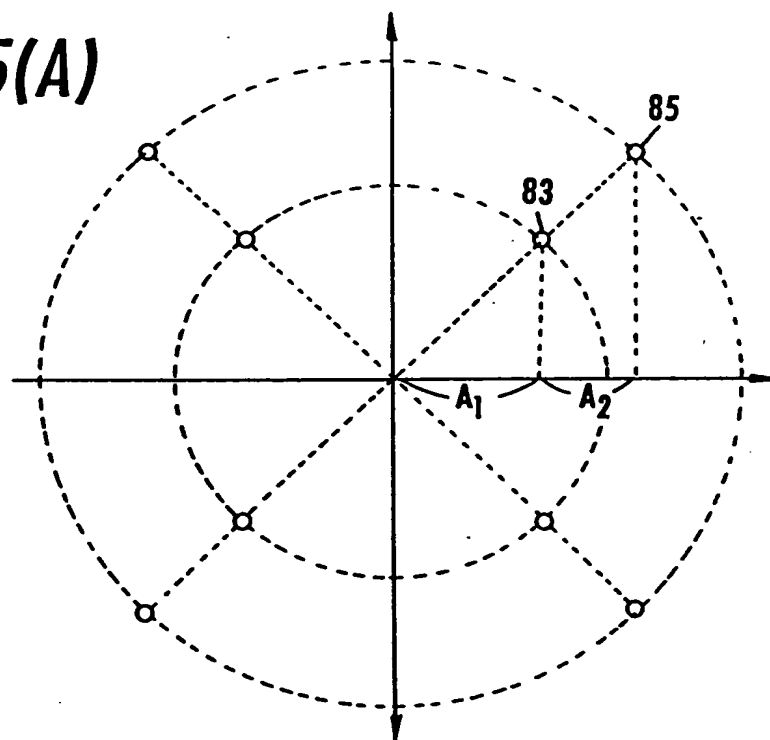


**FIG. 24**





**FIG. 25(A)**



**FIG. 25(B)**

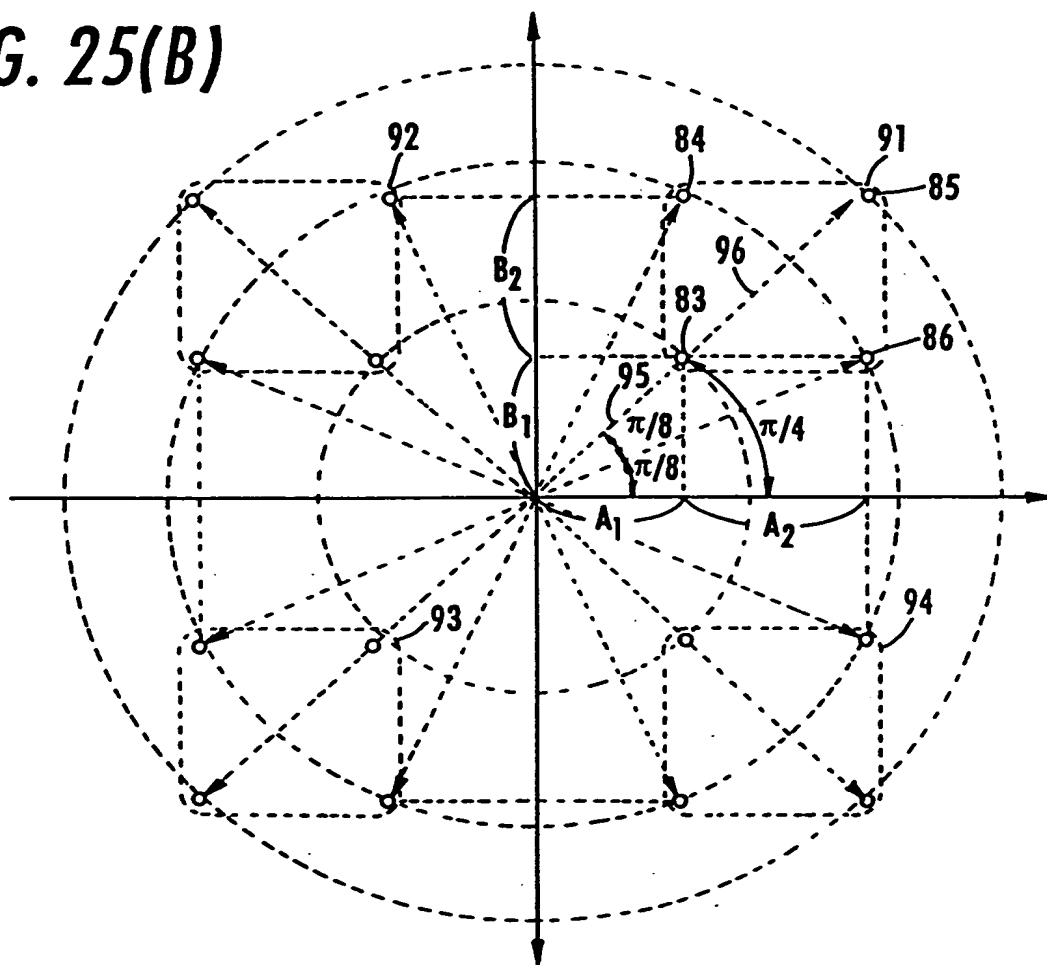


FIG. 26

2nd RECEIVER

DEMODULATOR

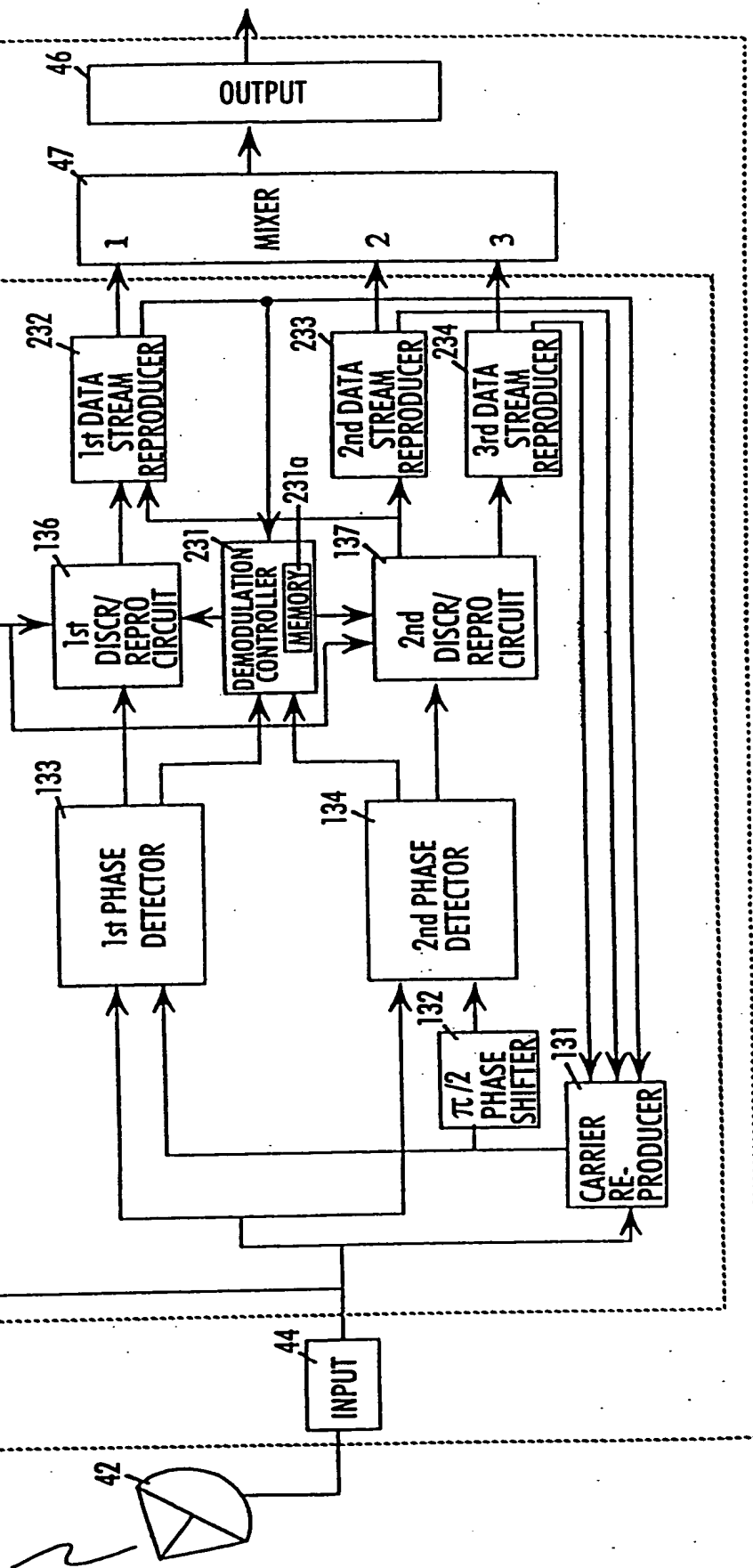
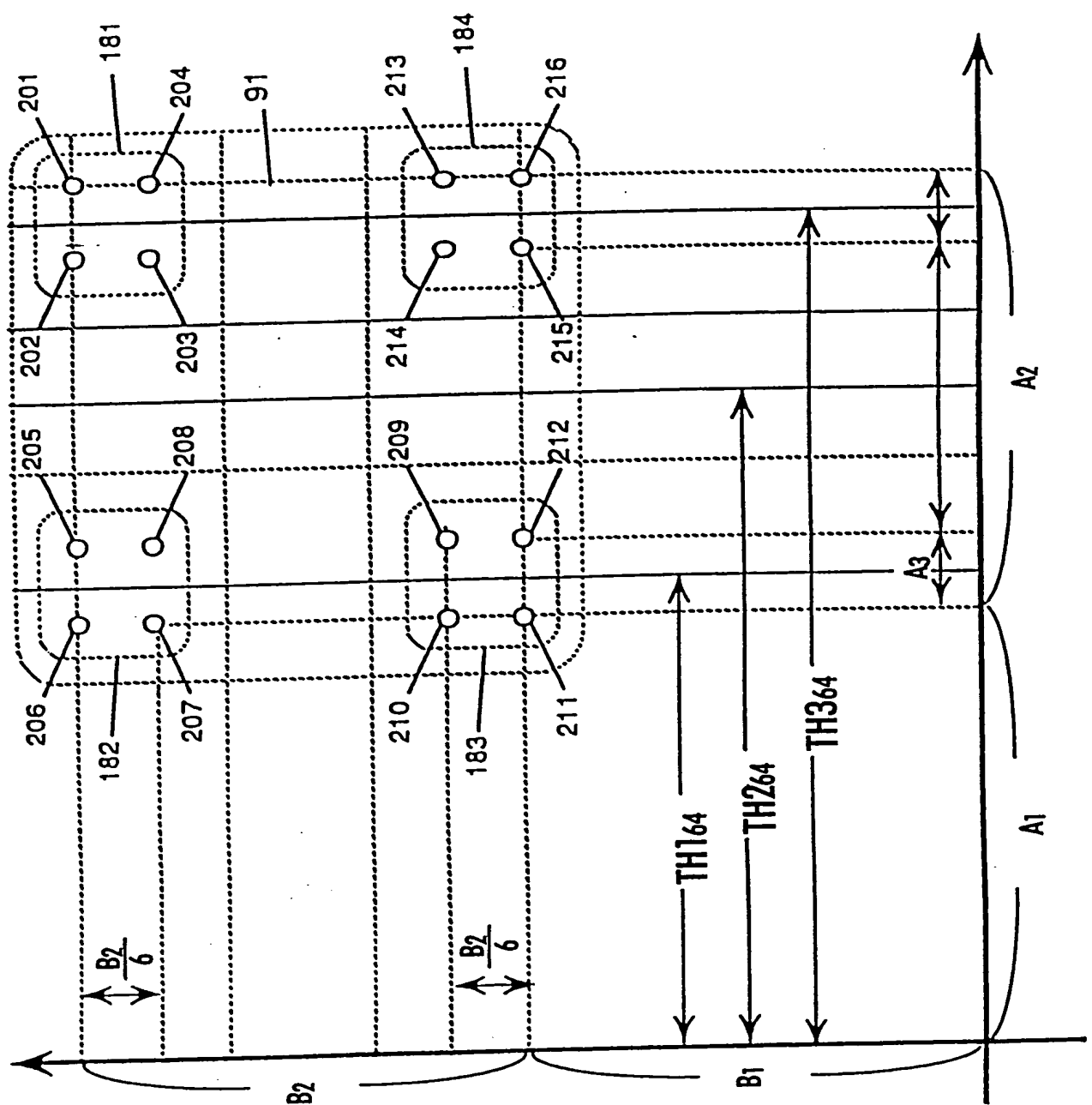
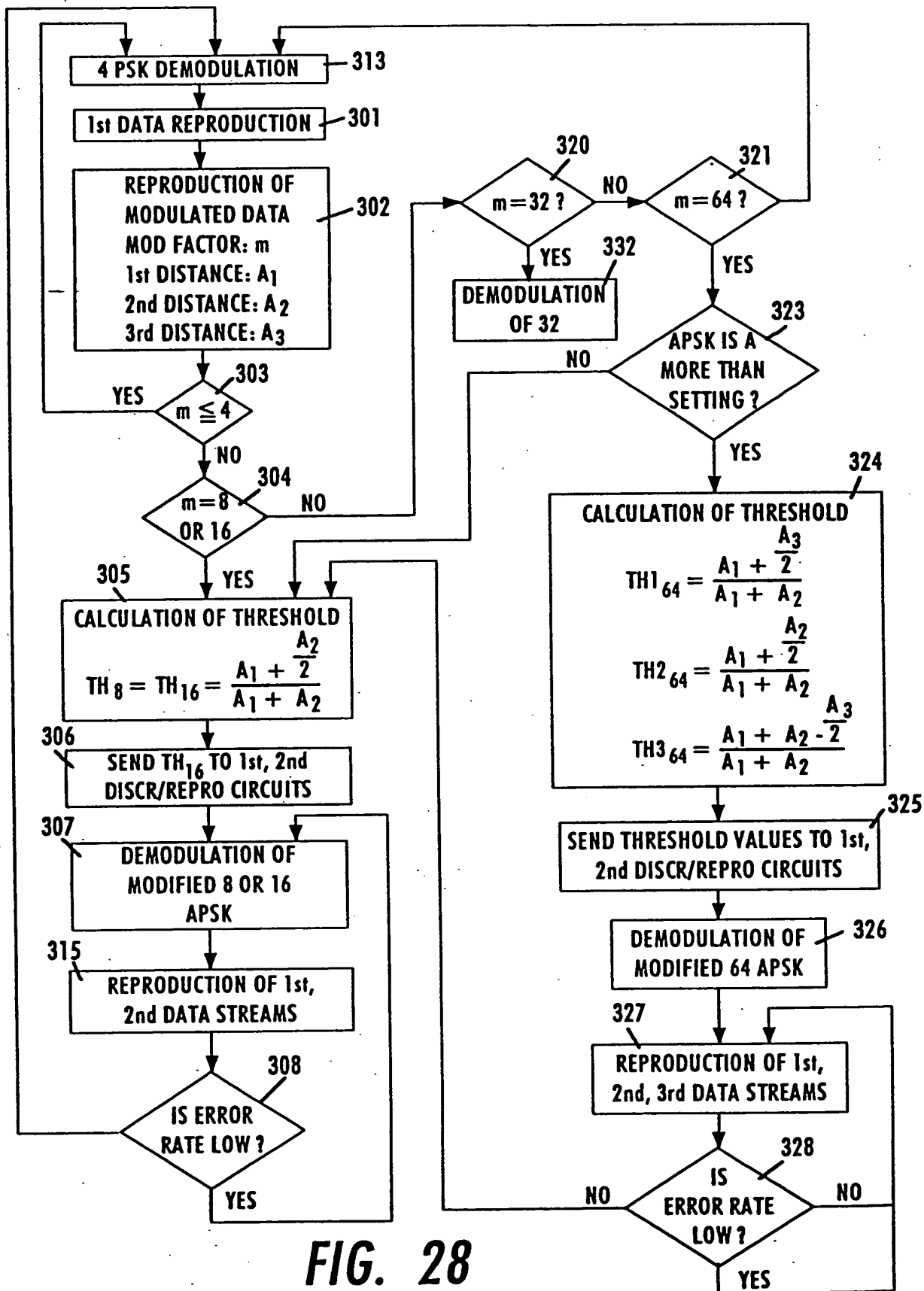


FIG. 27





**FIG. 28**

FIG. 29

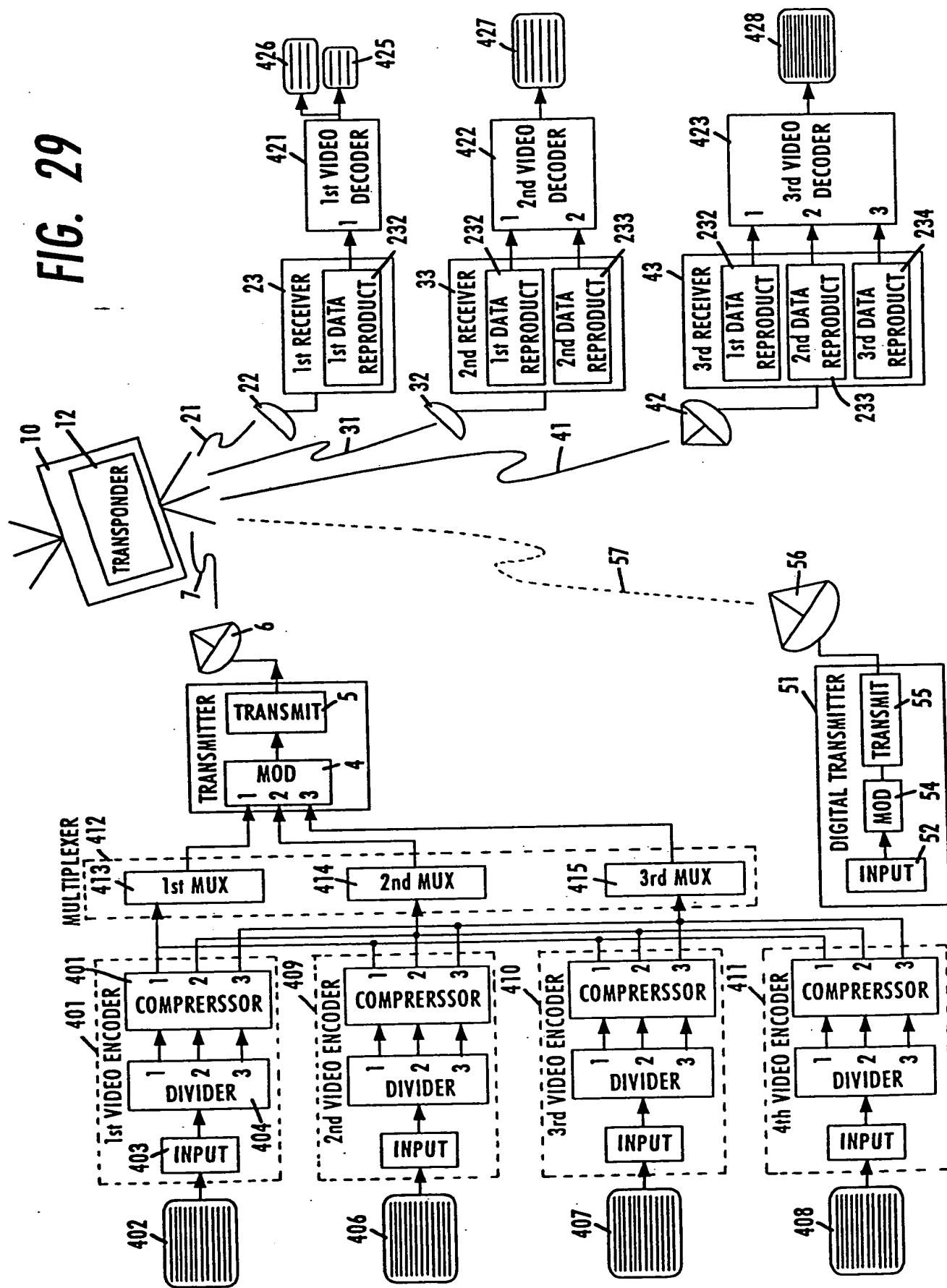


FIG. 30

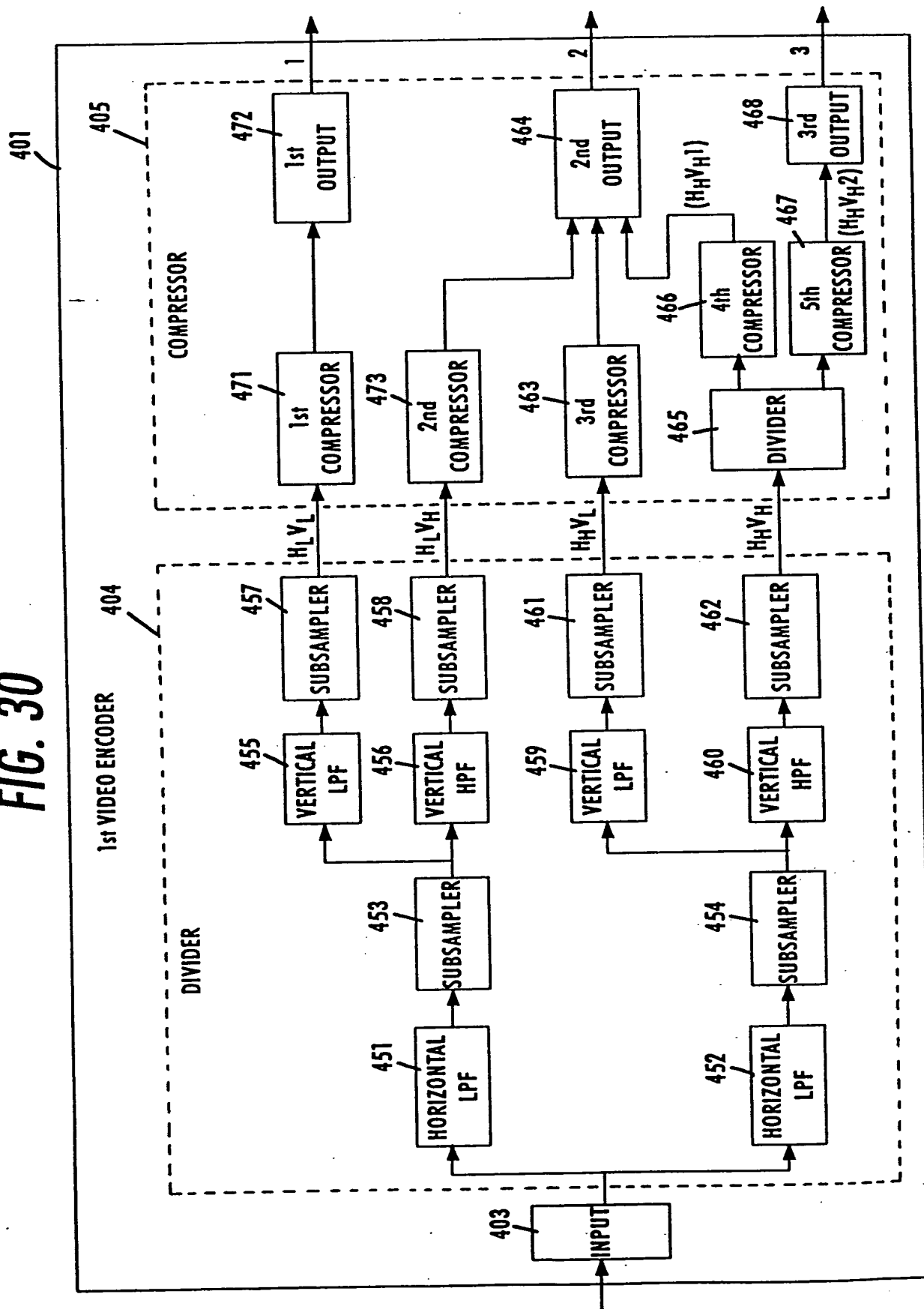


FIG. 31

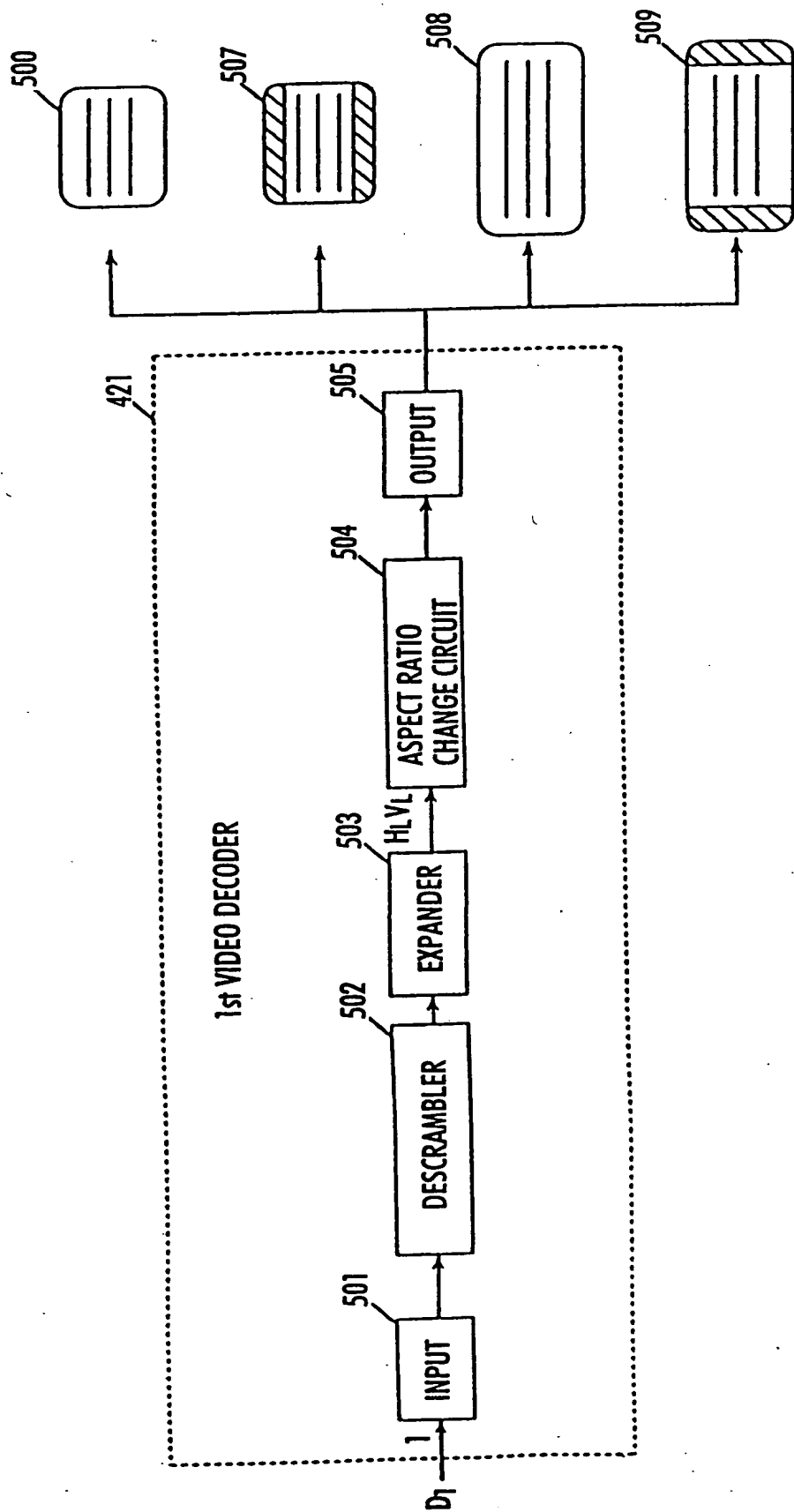
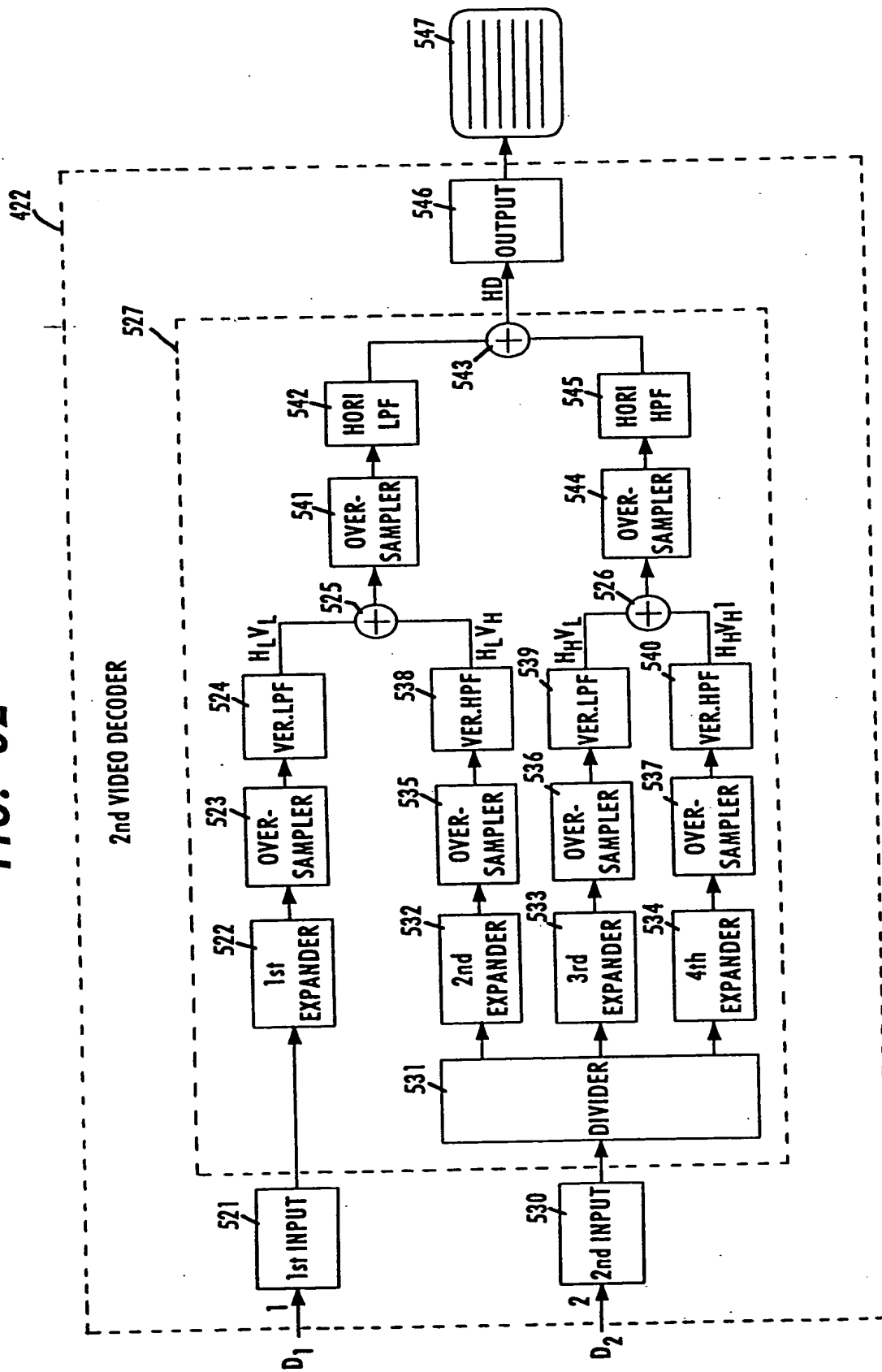


FIG. 32





423

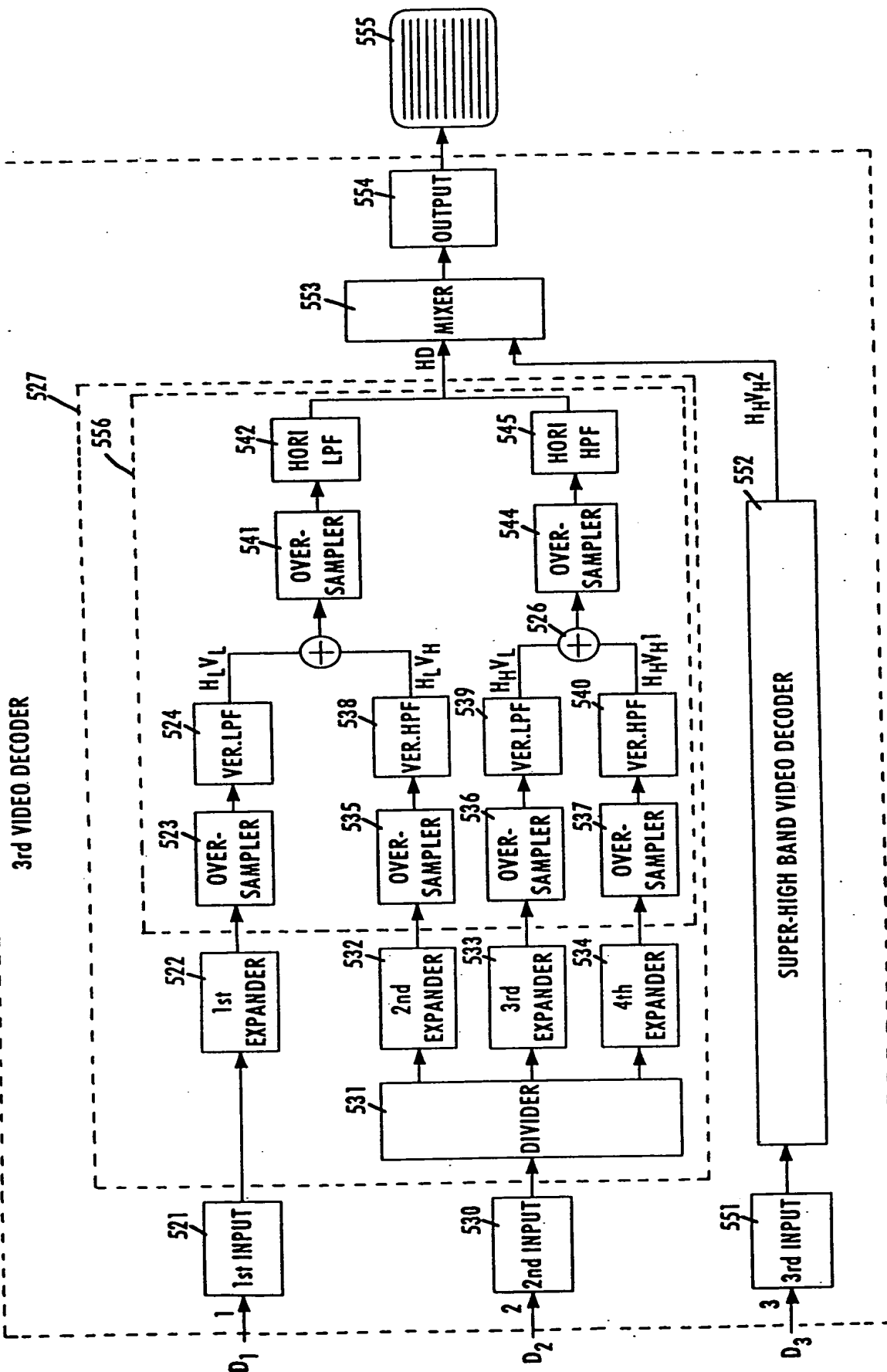


FIG. 34

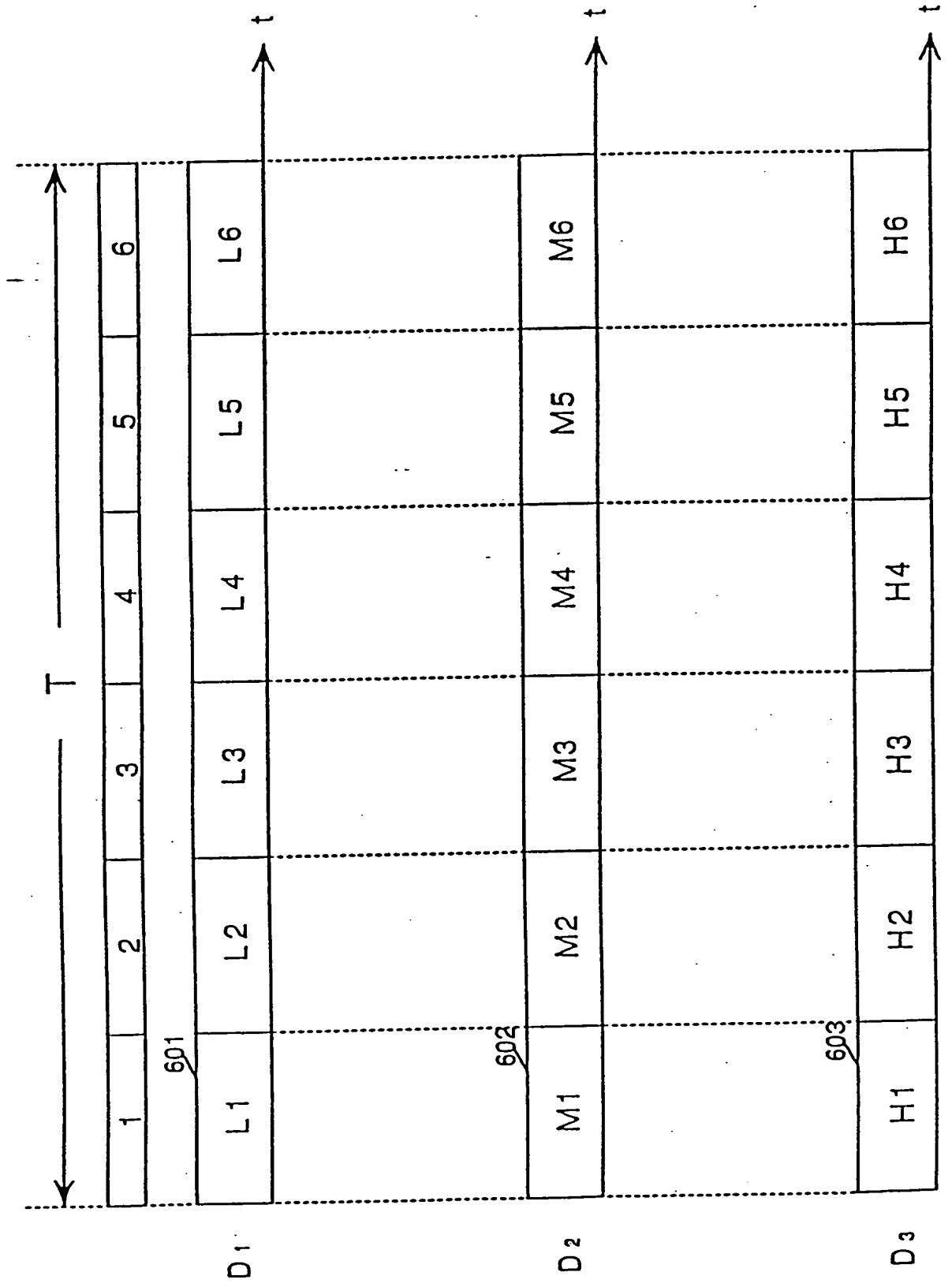


FIG. 35

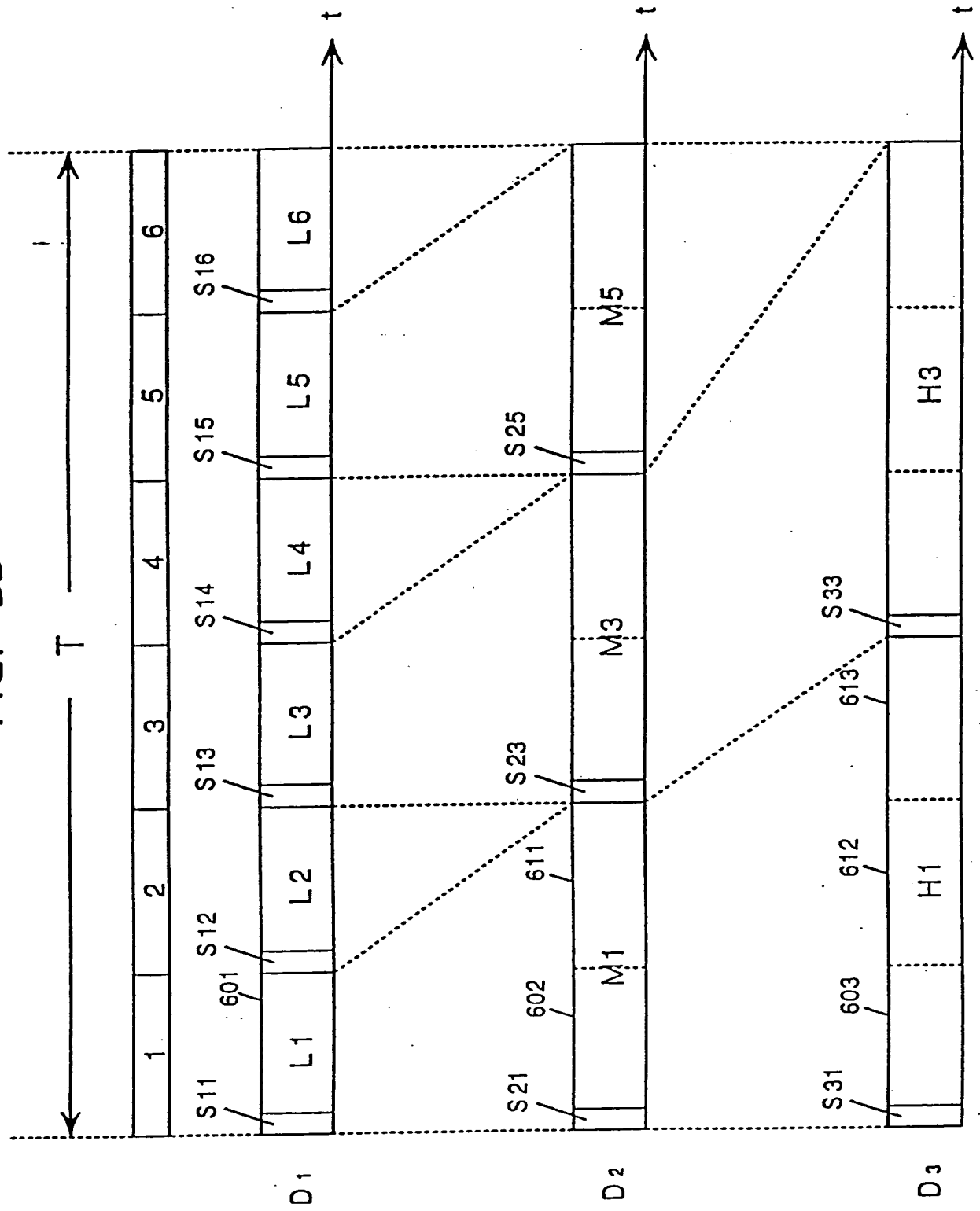


FIG. 36

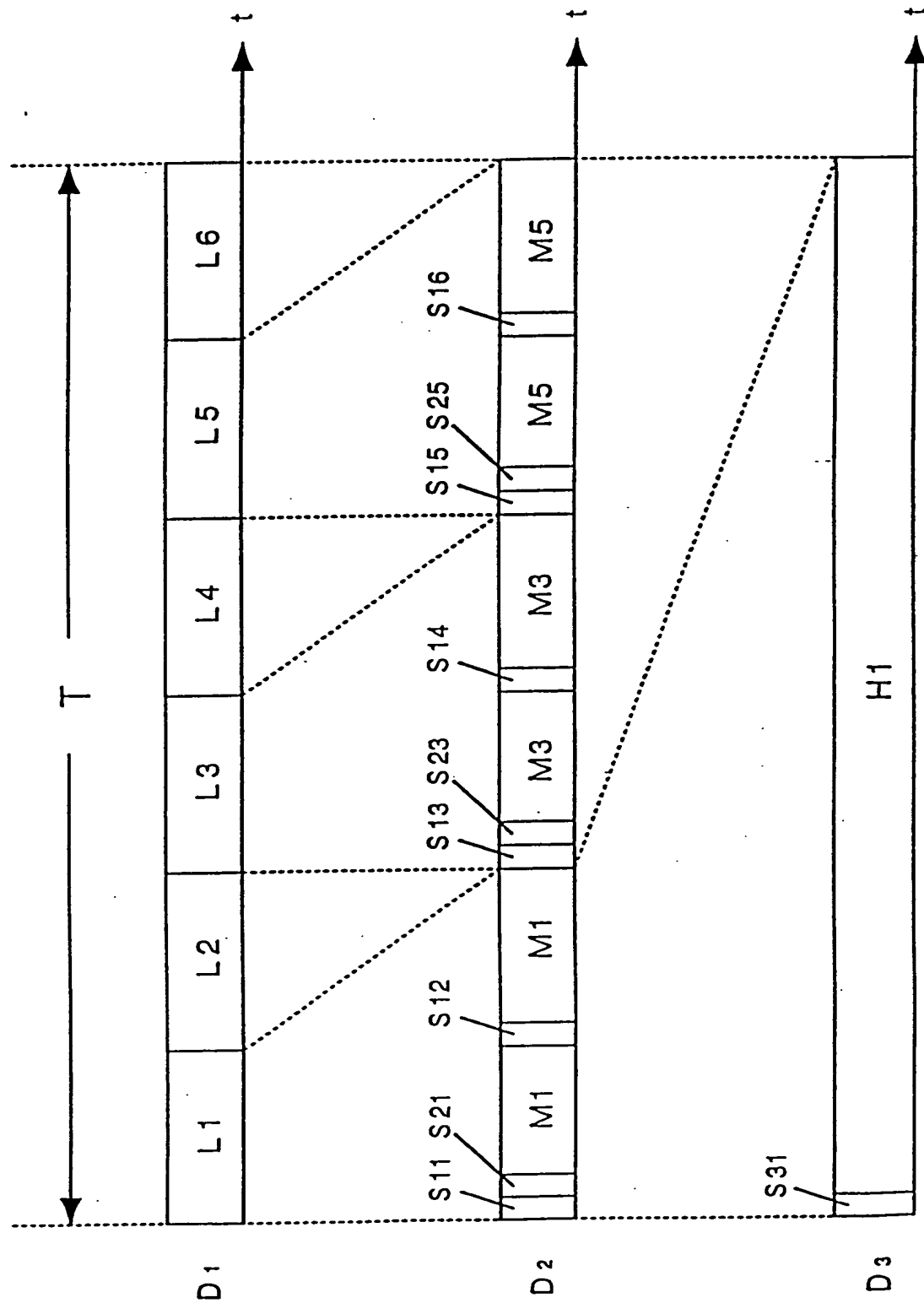


FIG. 37

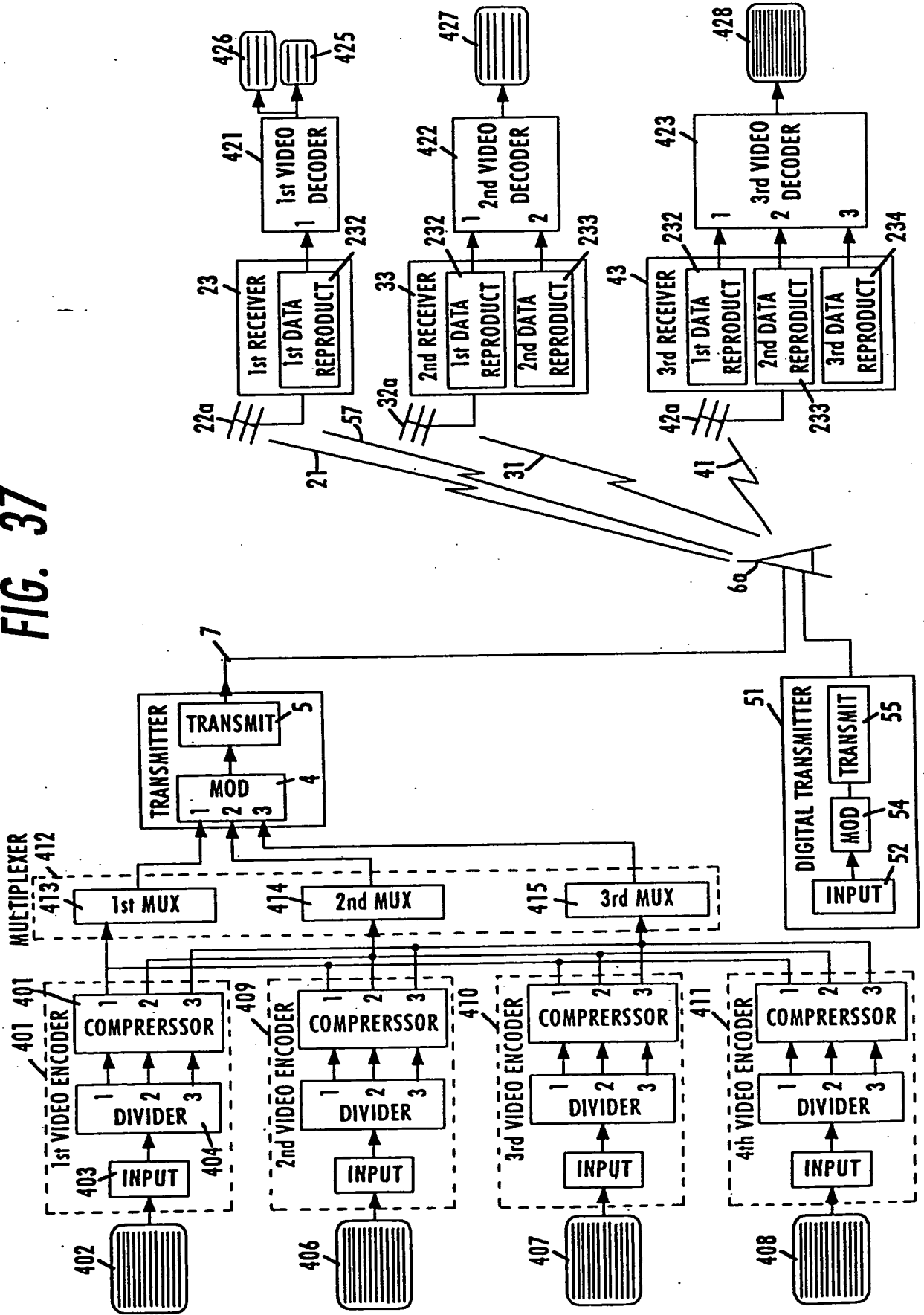
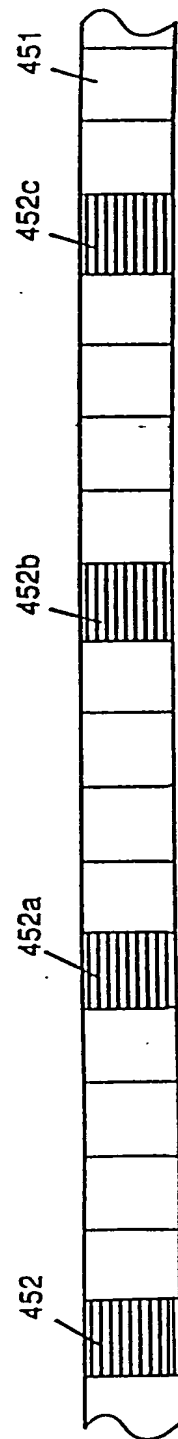
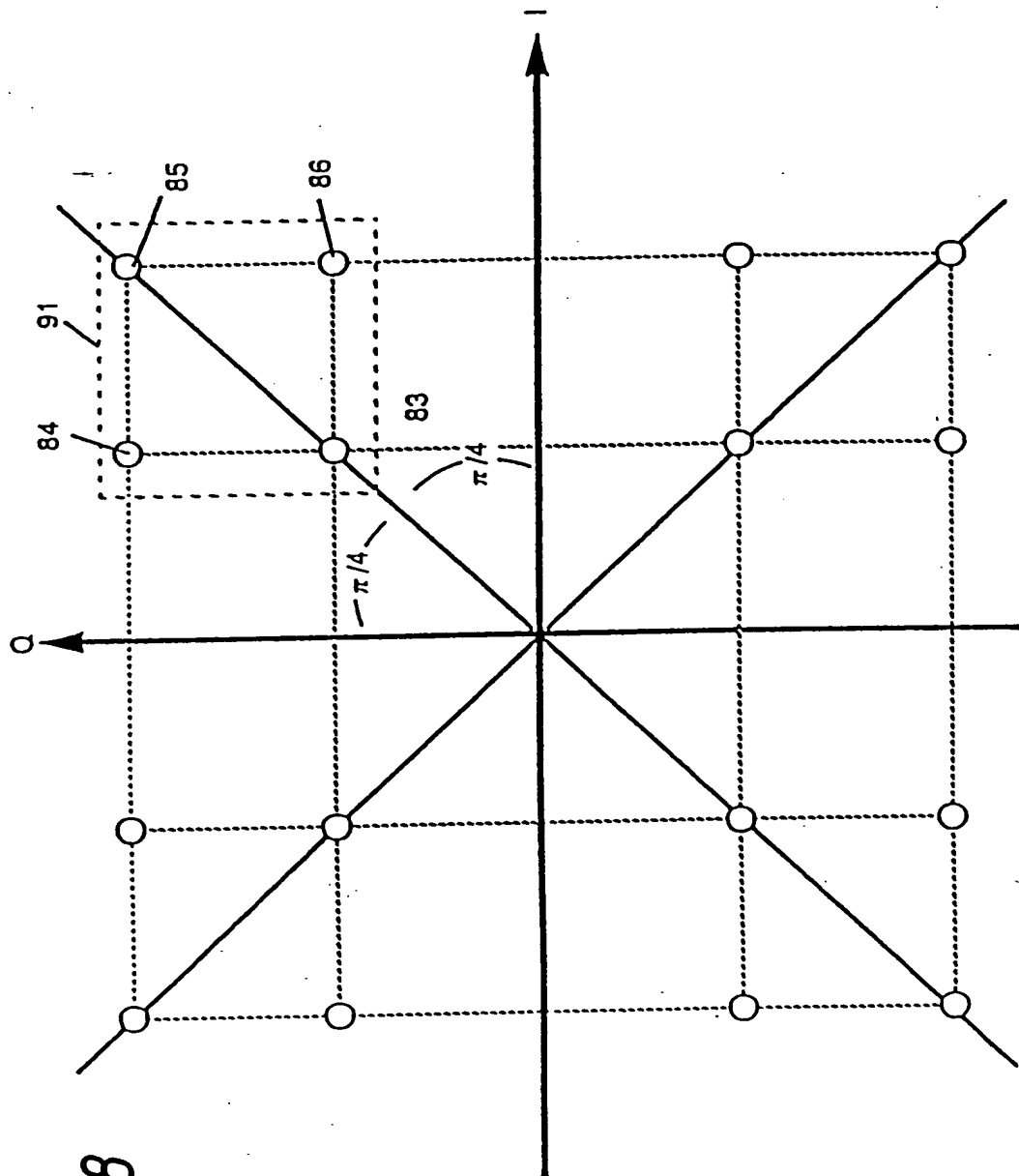
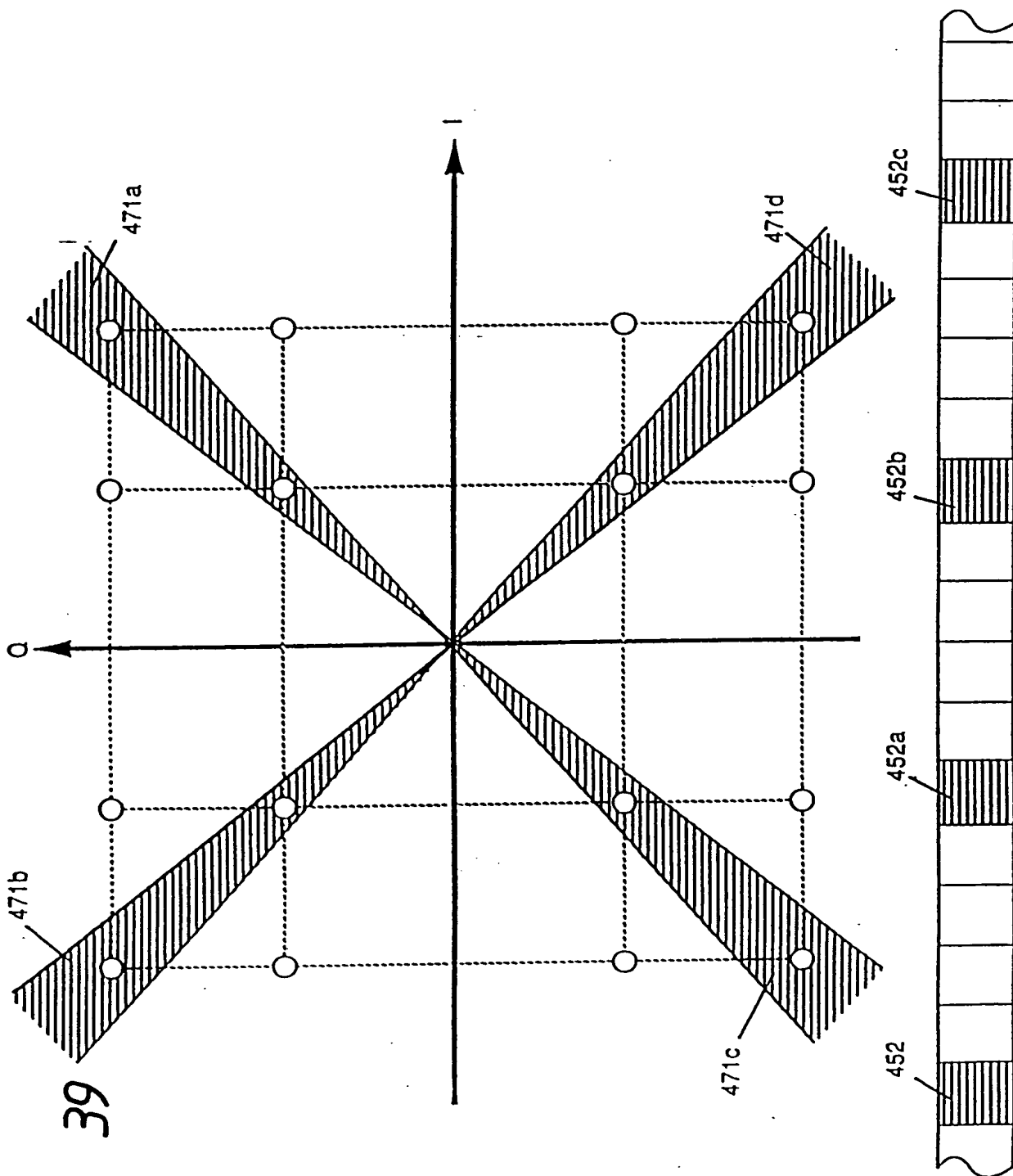
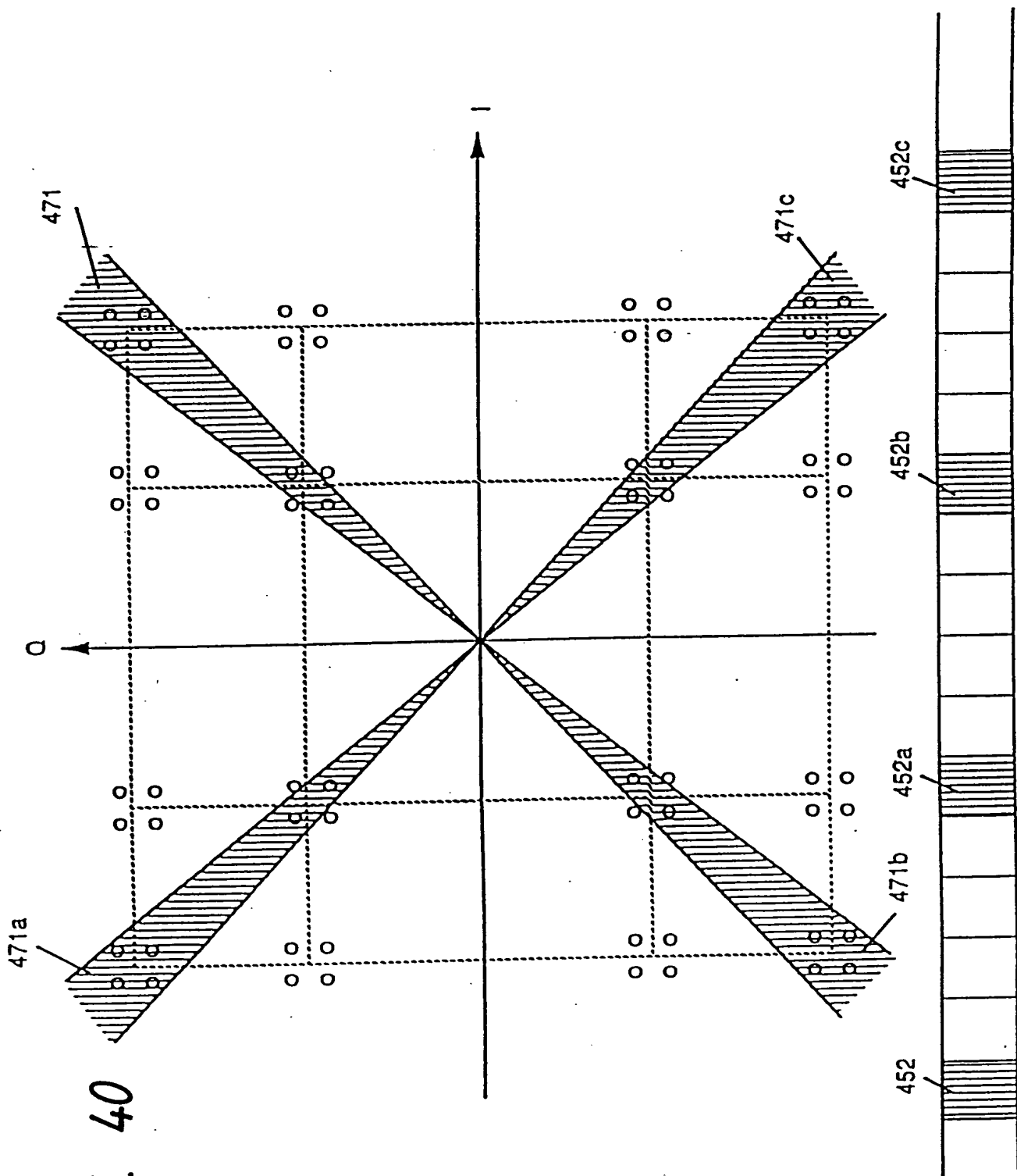


FIG. 38









The diagram illustrates a frame structure and its components. The main part shows a horizontal bar divided into segments labeled S, Ib, D<sub>1</sub>, D<sub>2</sub>, D<sub>3</sub>, and D<sub>n</sub>. Above this bar are two detailed views of segments: one showing S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>, H, and I; another showing S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>, H, and I. To the right, a vertical bar is shown with segments G, S, D<sub>1</sub>, D<sub>2</sub>, D<sub>3</sub>, D<sub>4</sub>, and D<sub>n</sub>. Below the main bar, a small box contains S<sub>1</sub>, S<sub>2</sub>, S<sub>3</sub>, H, and I. Arrows indicate dimensions t and FRAME.

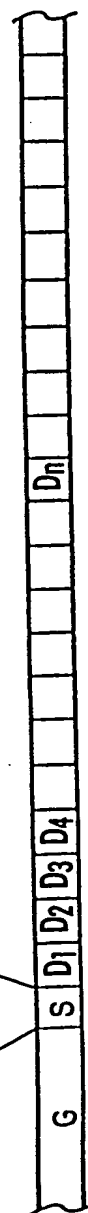


FIG. 42

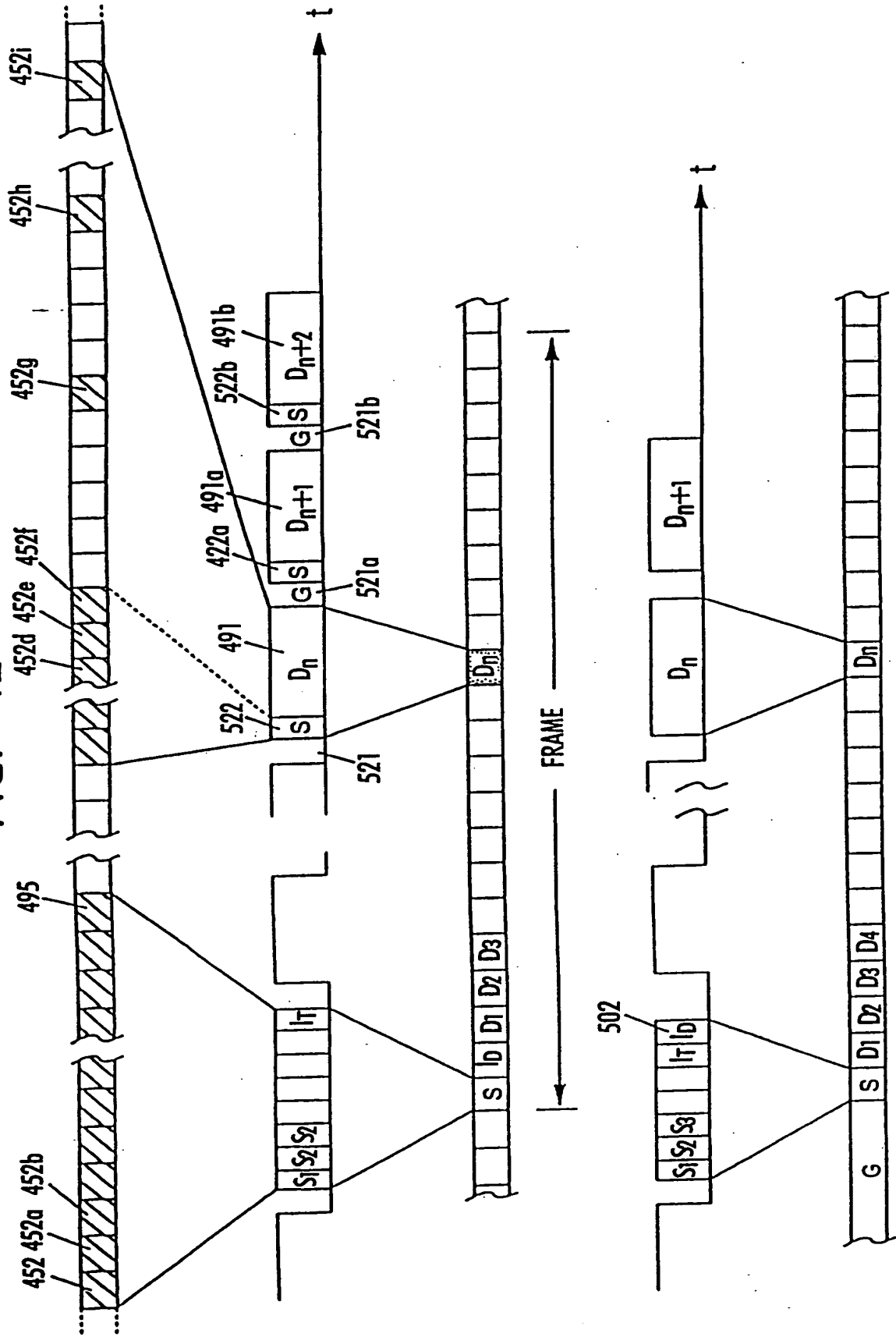


FIG. 43

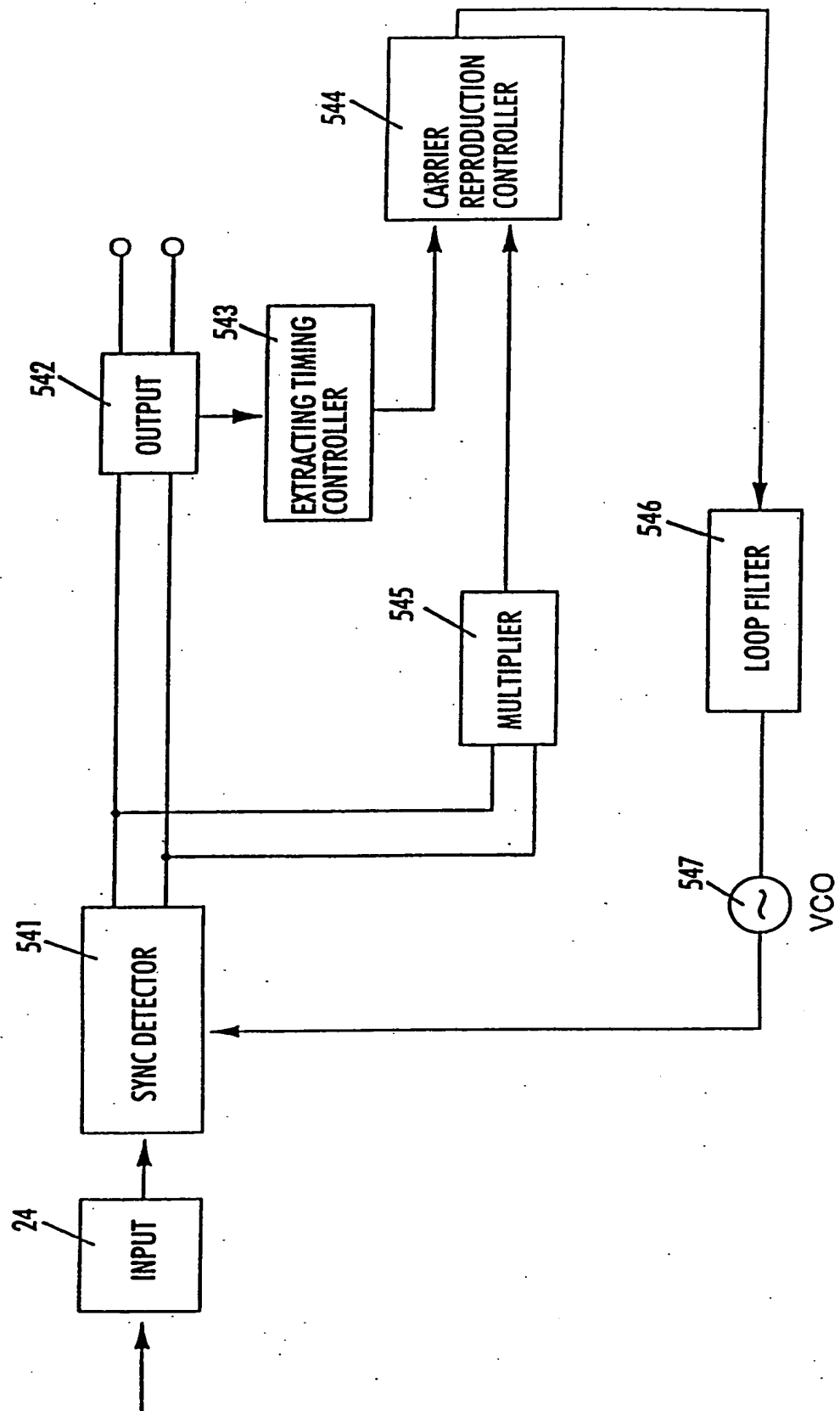


FIG. 44

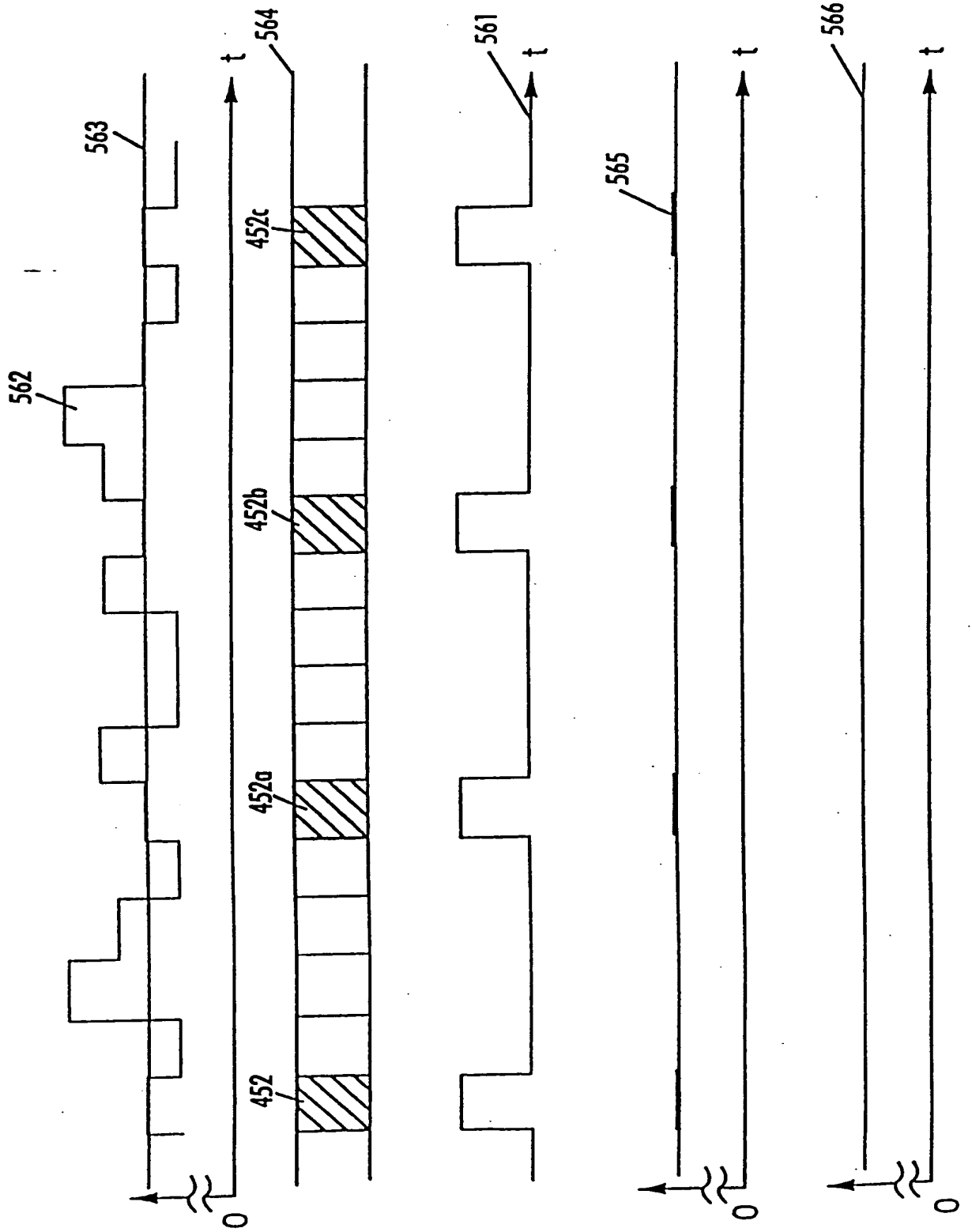


FIG. 45

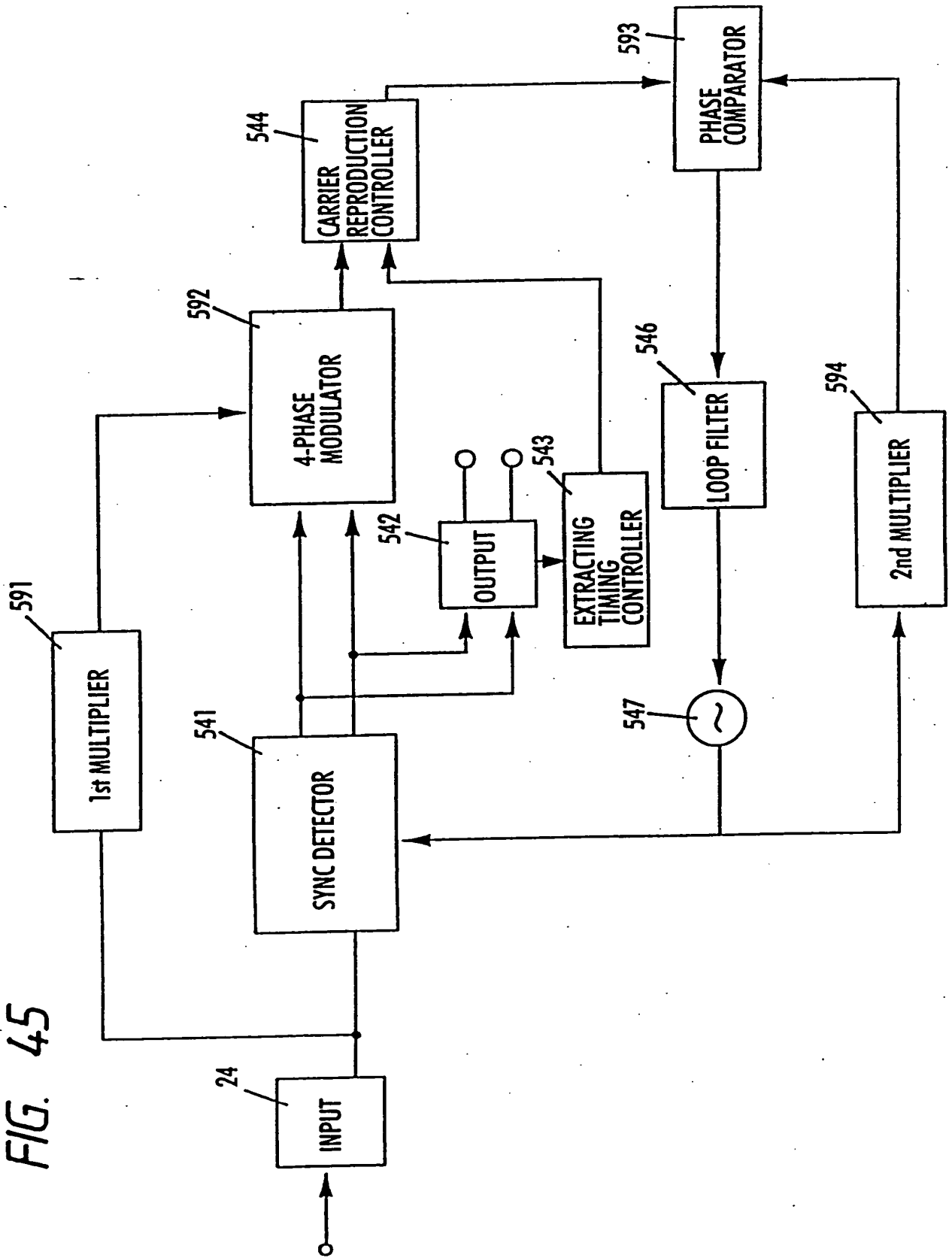


FIG. 46

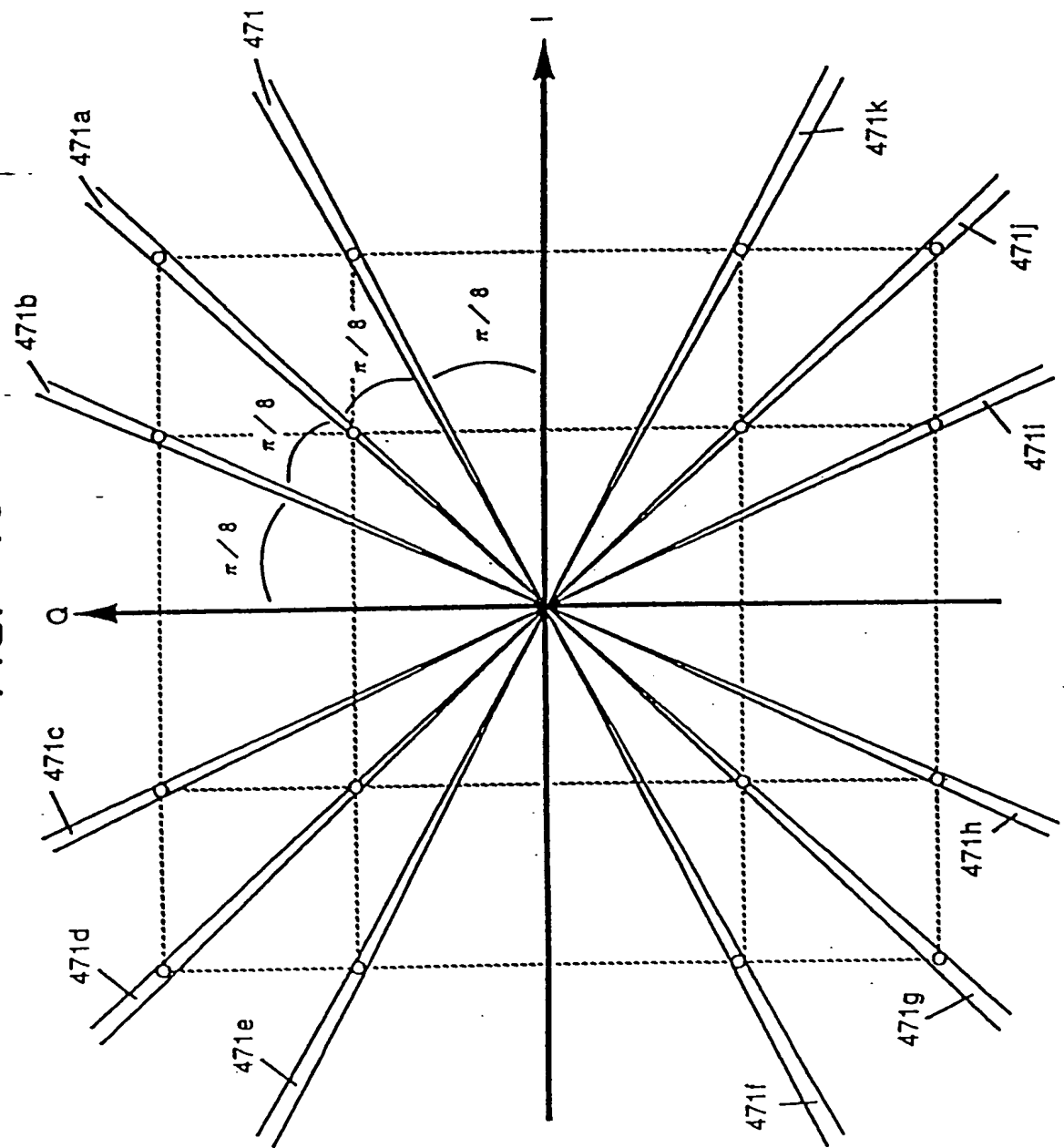


FIG. 47

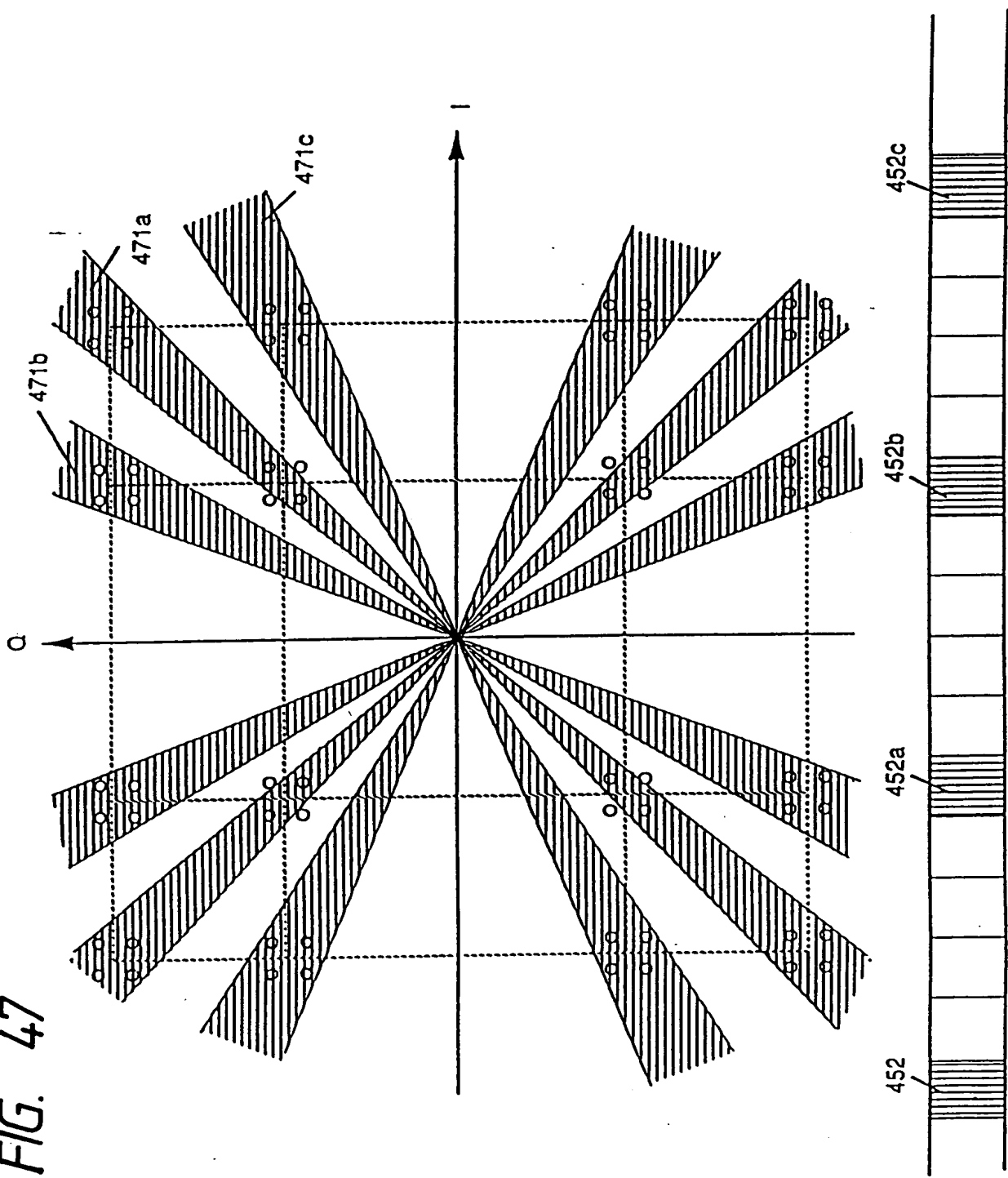


FIG. 48

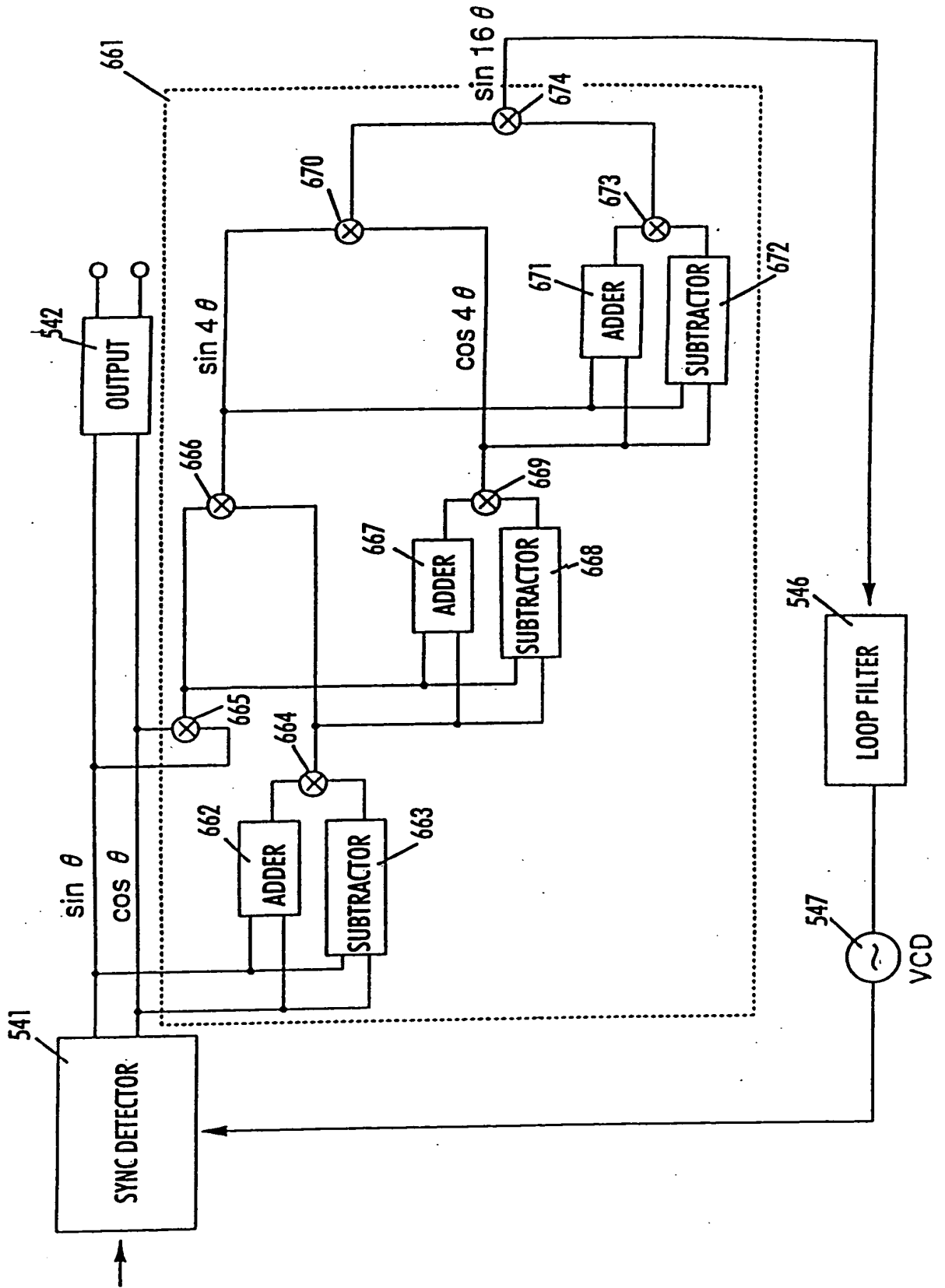




FIG. 49

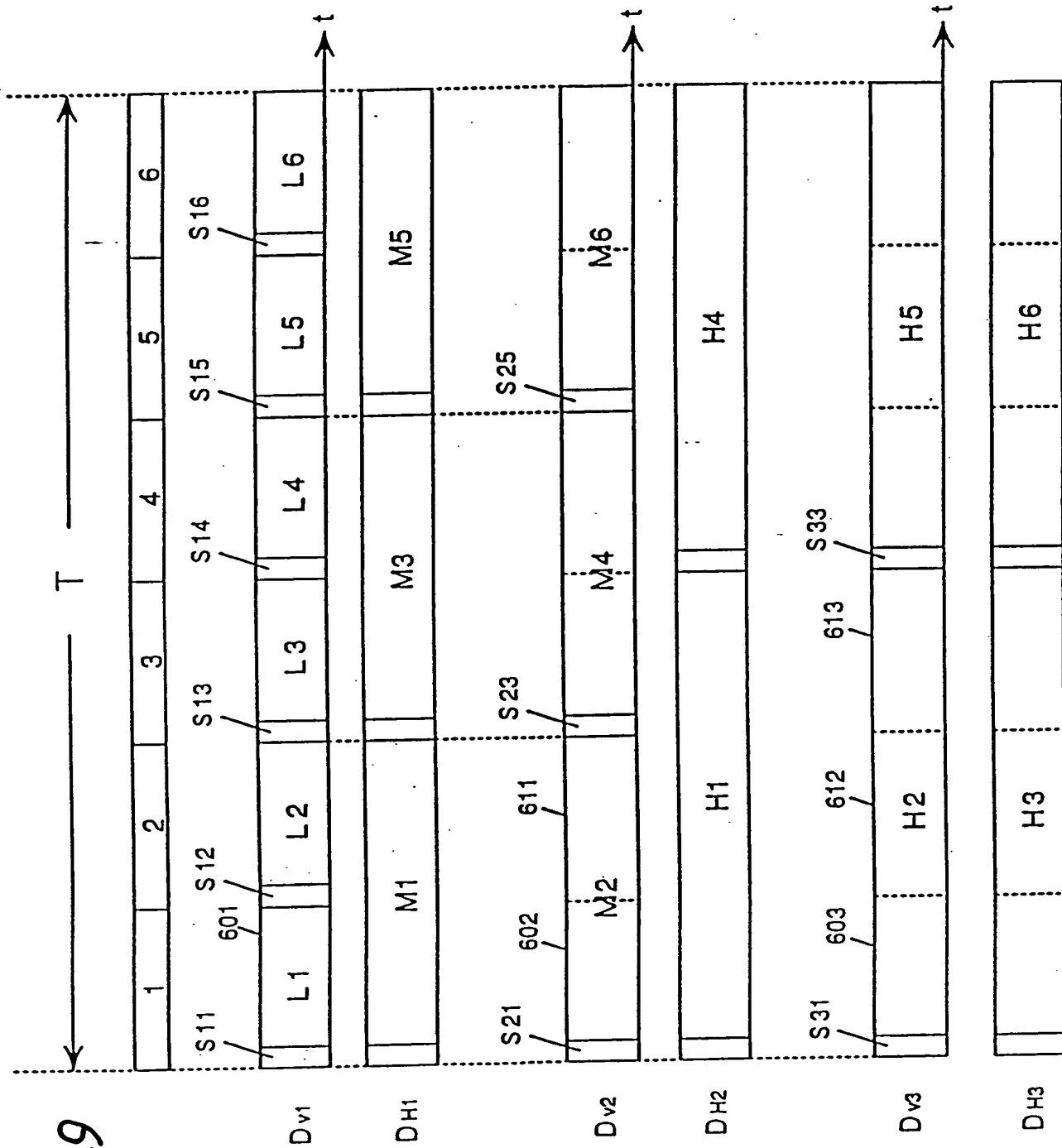


FIG. 50

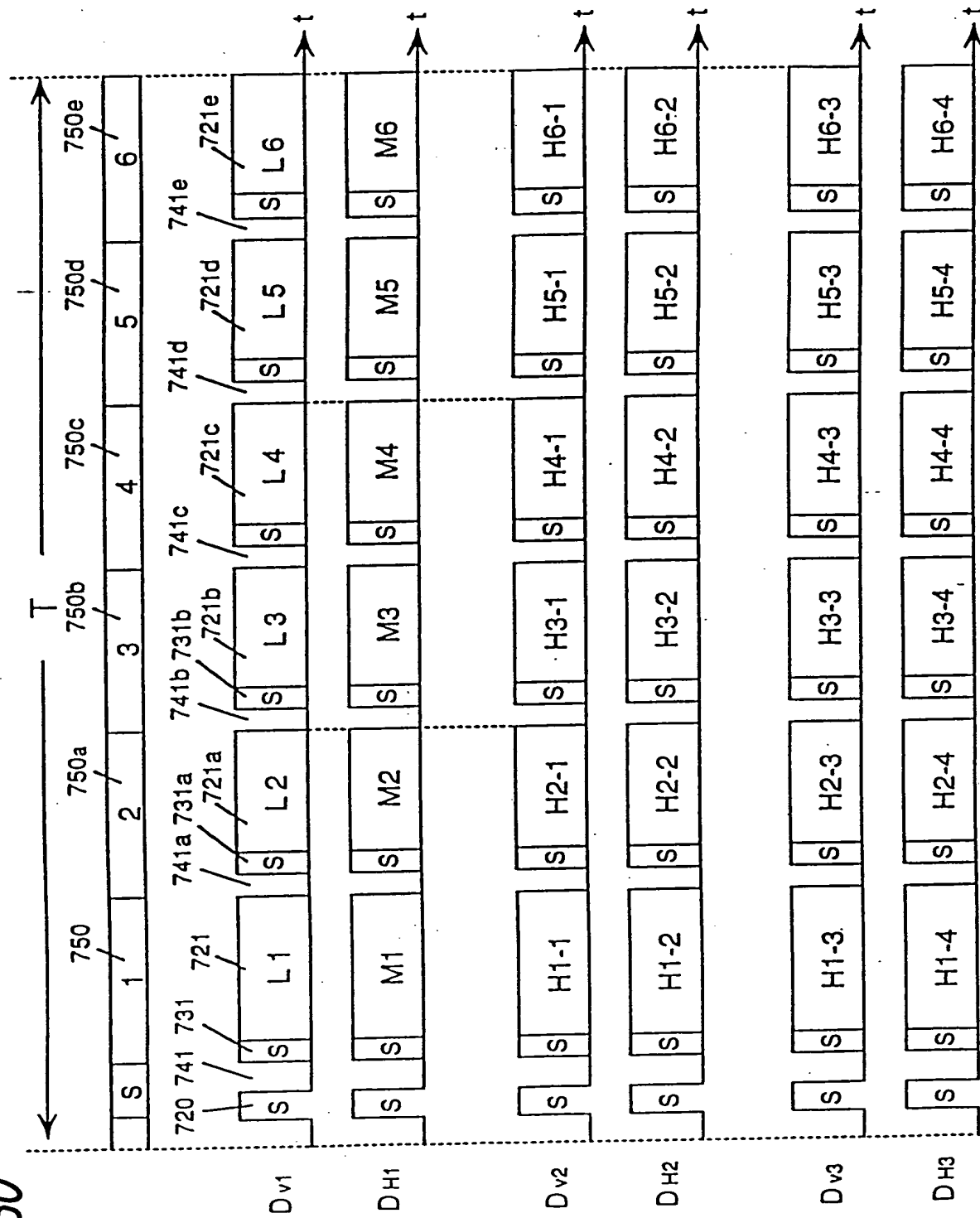


FIG. 51

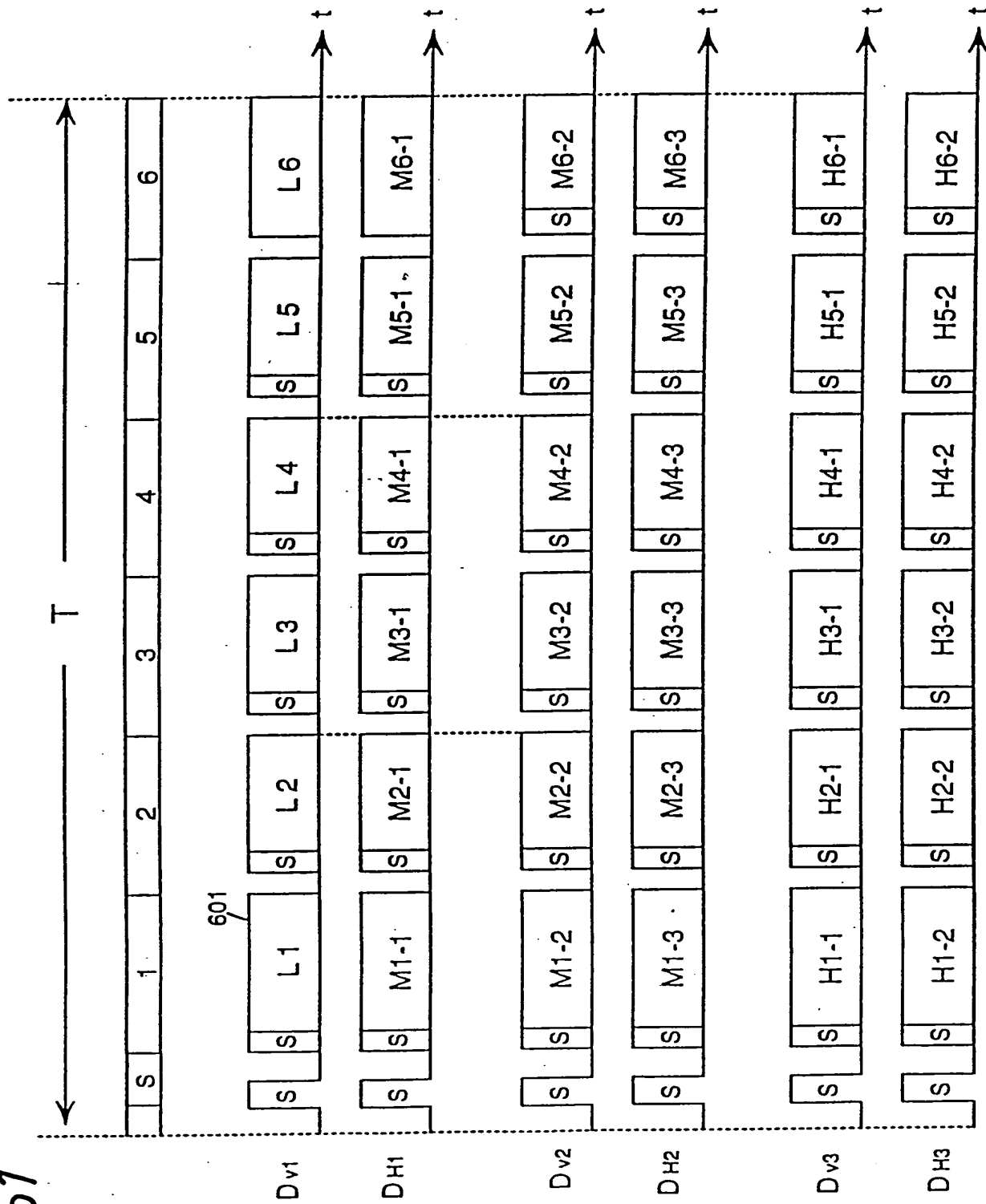


FIG. 52

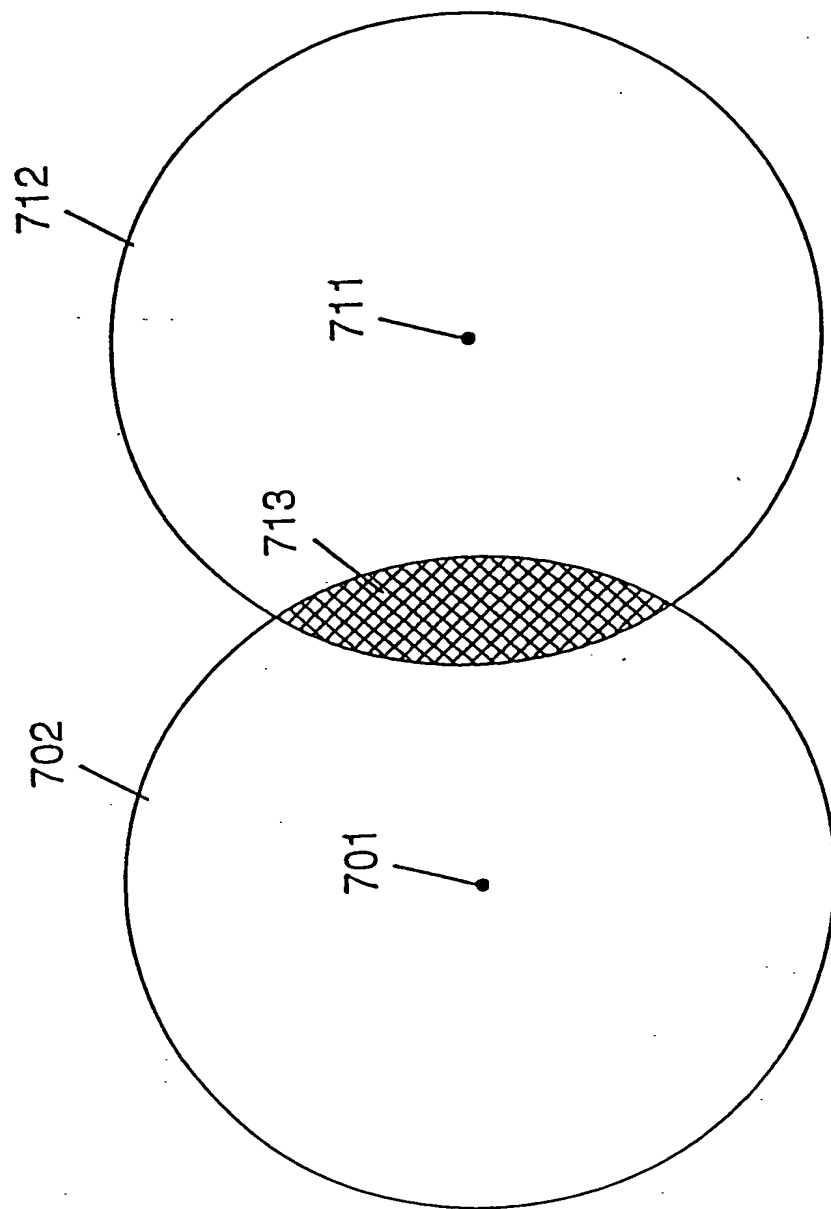


FIG. 53

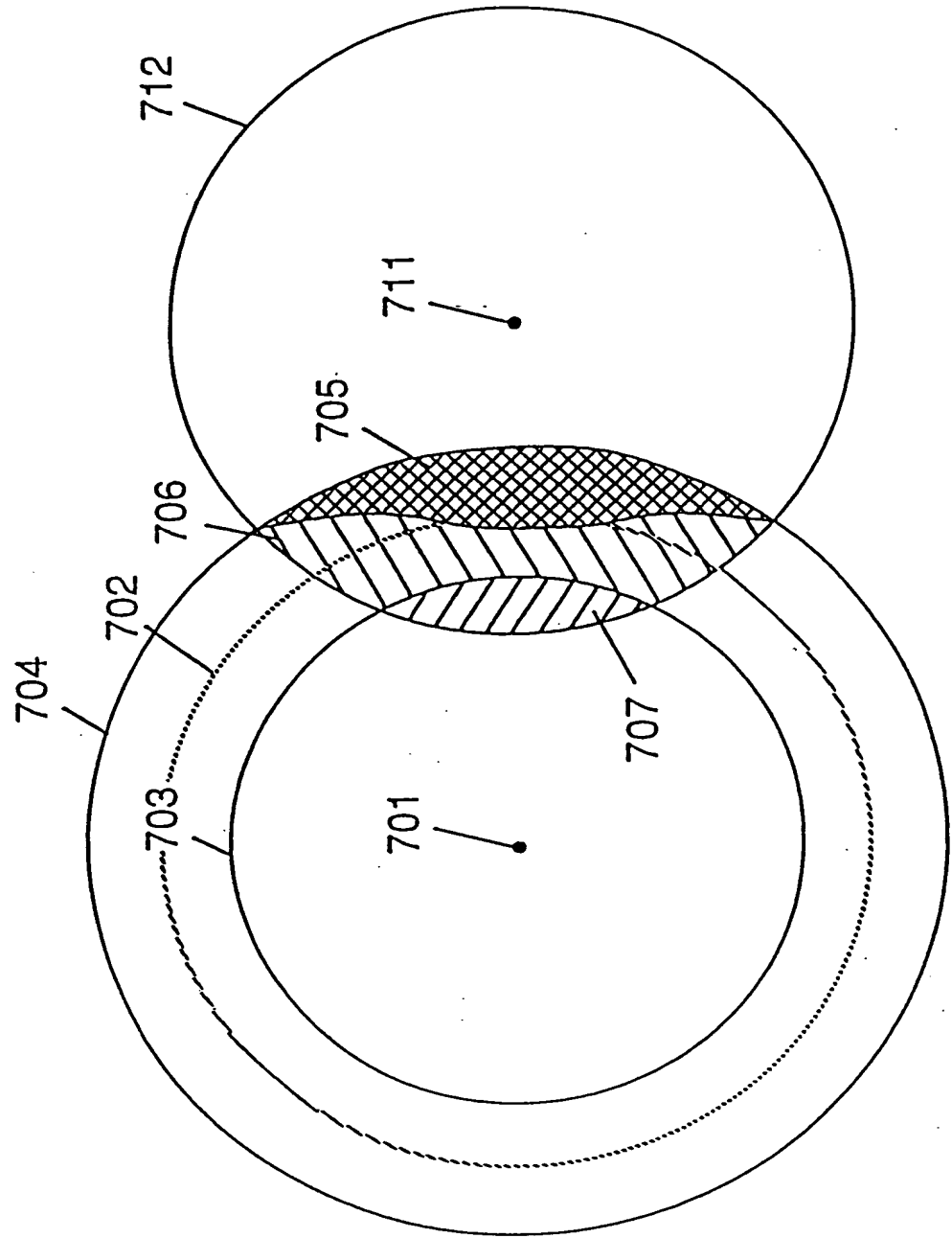


FIG. 54

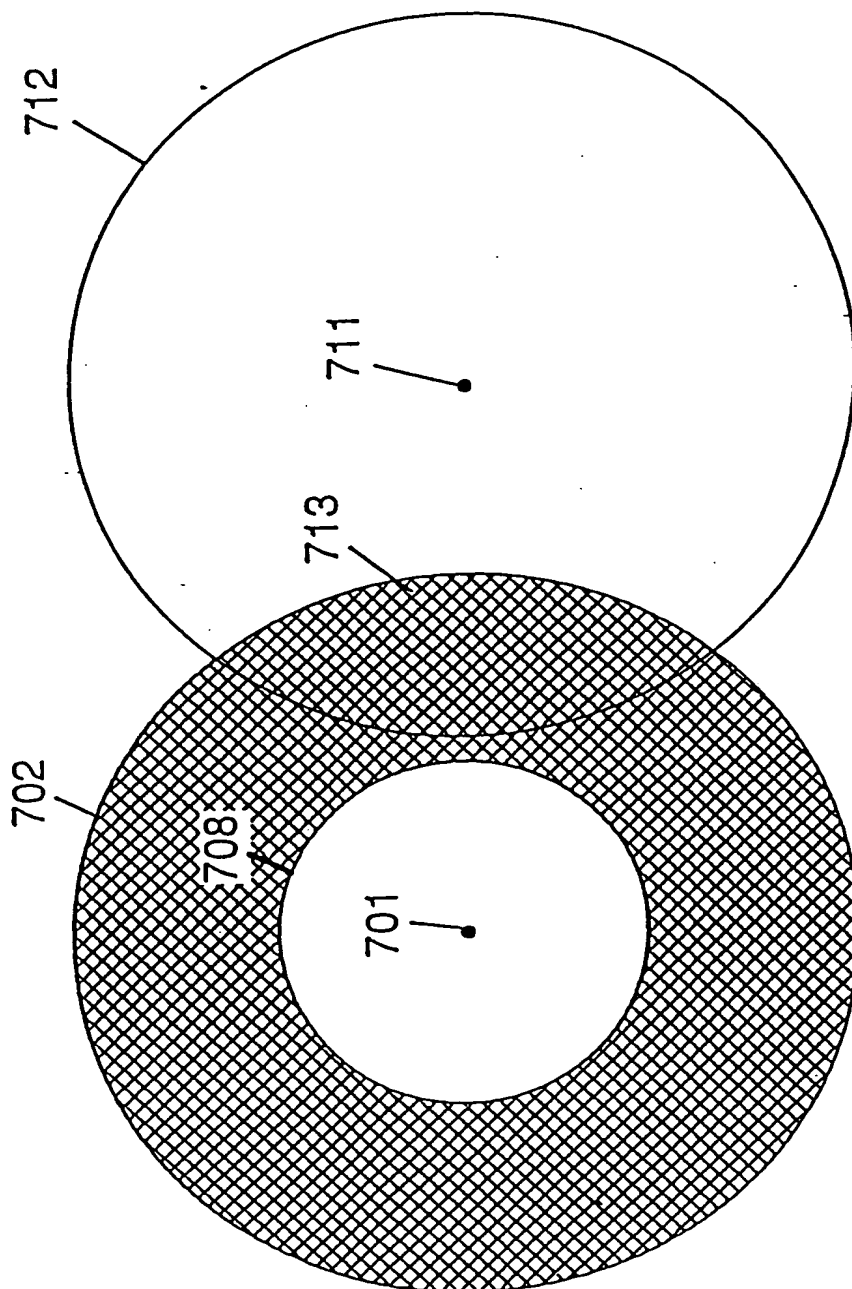


FIG. 55

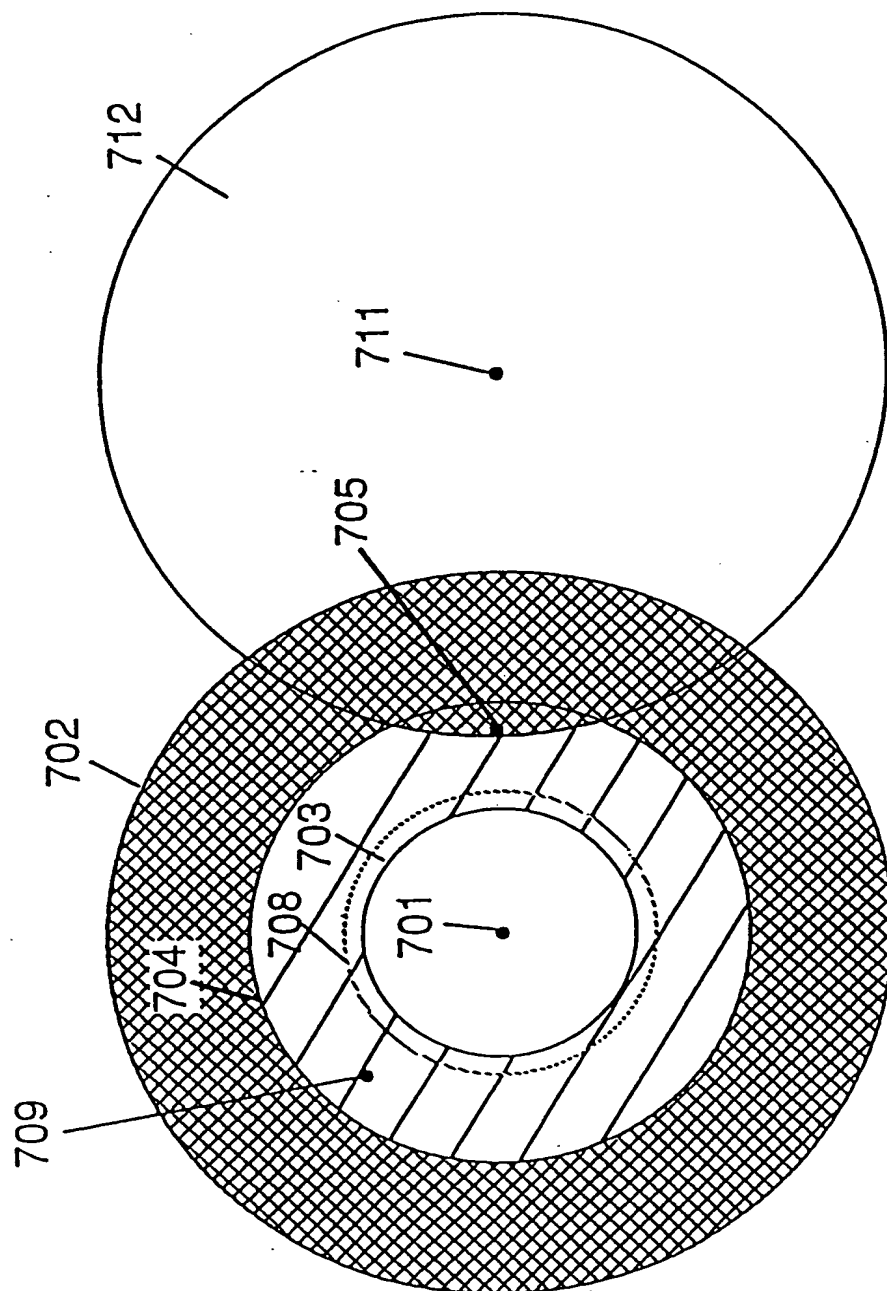


FIG. 56

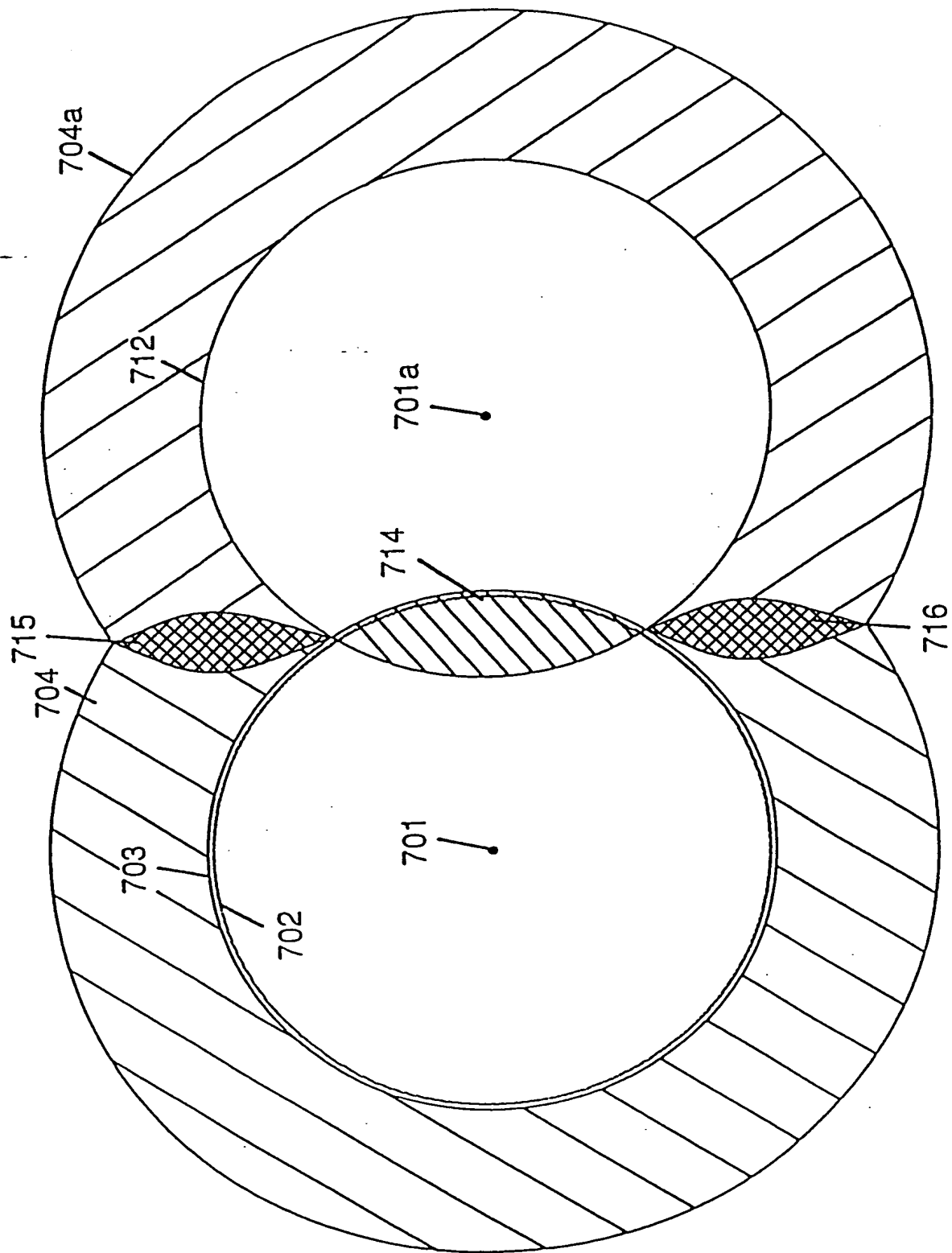




FIG. 57

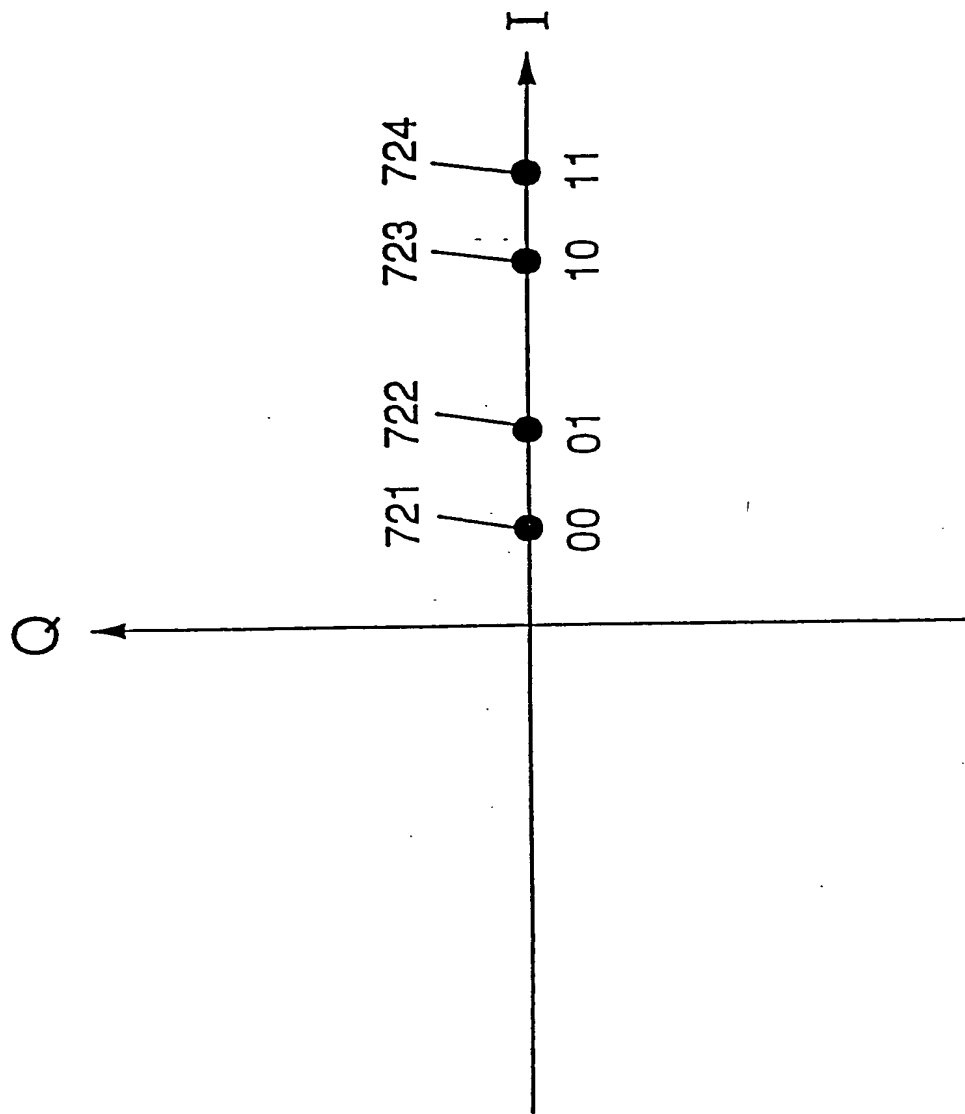


FIG. 58

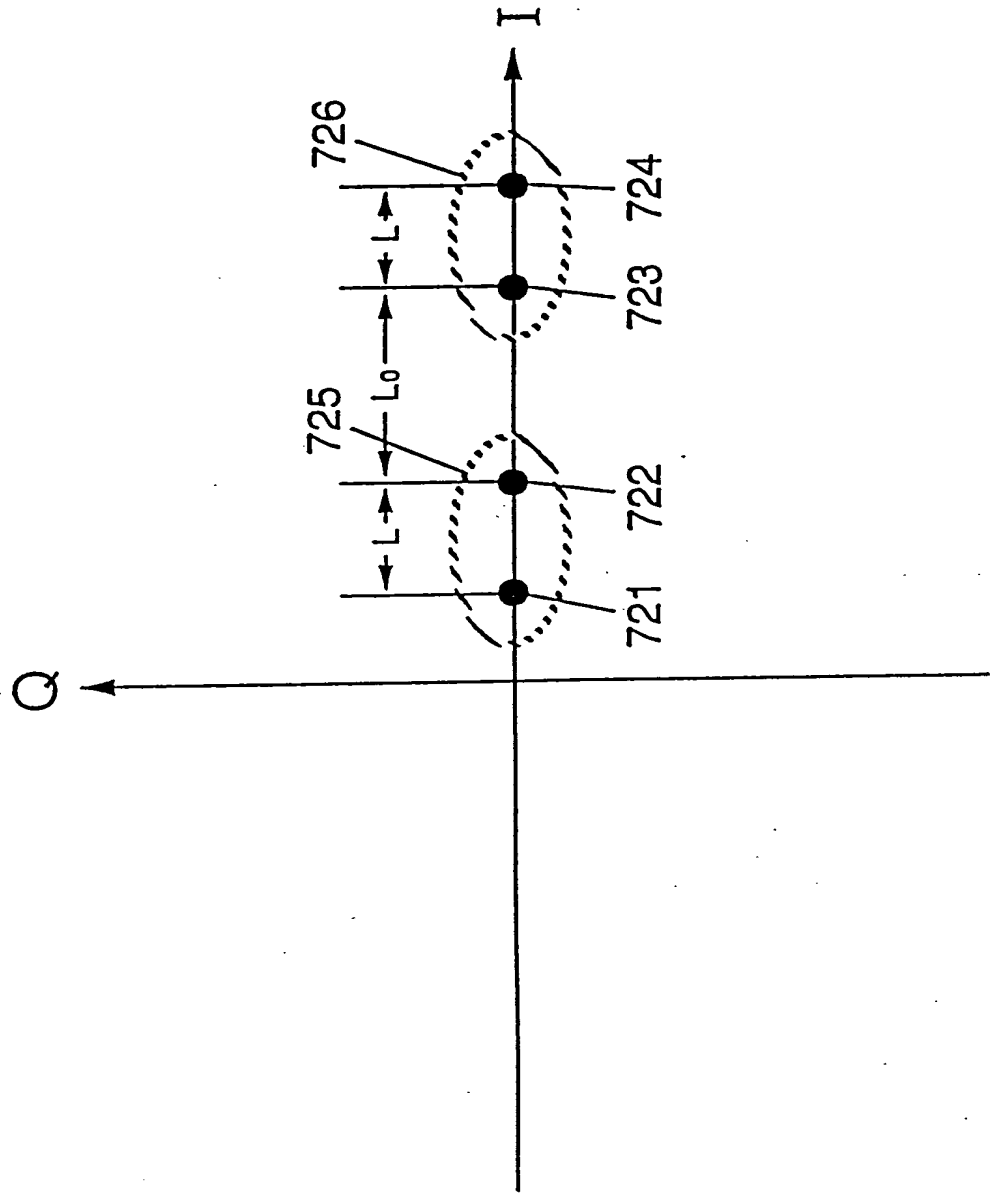


FIG. 59(a)

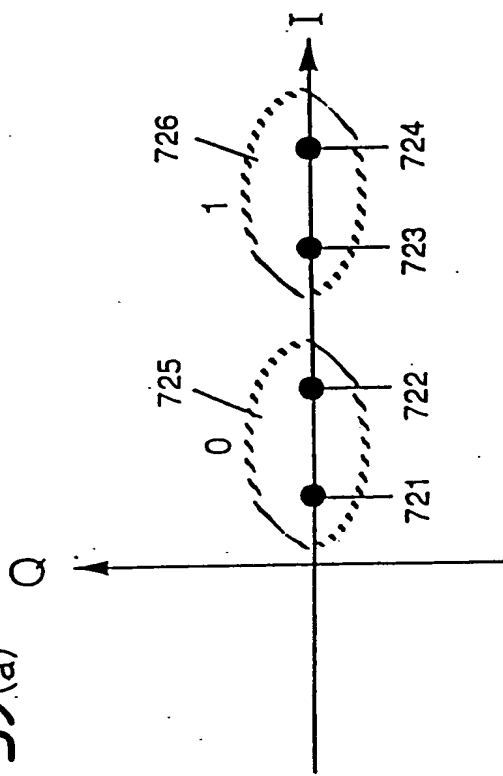


FIG. 59(c)

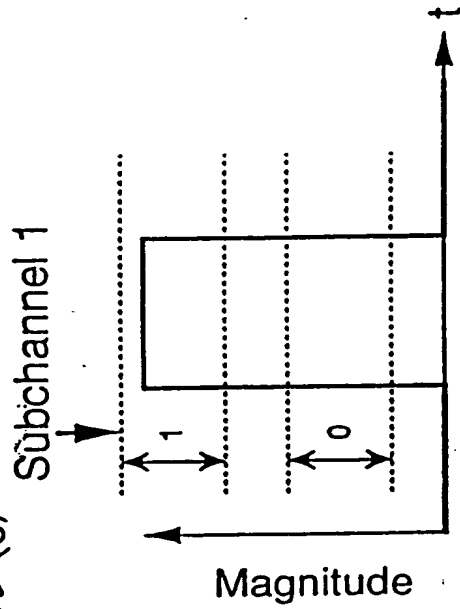


FIG. 59(b)

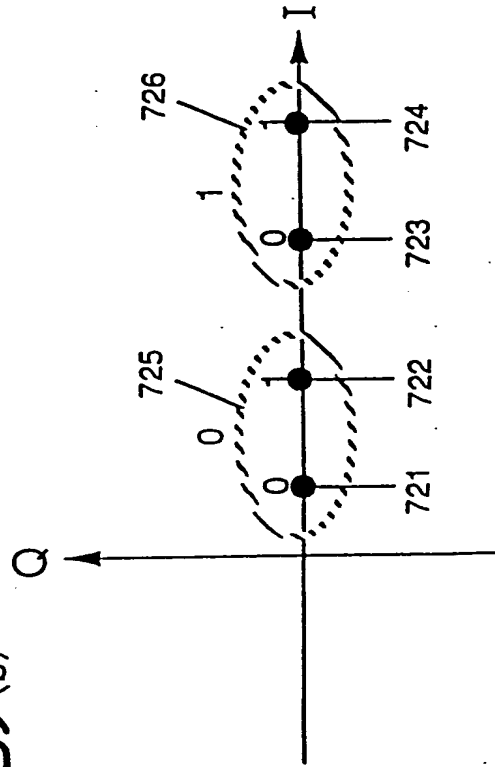


FIG. 59(d)

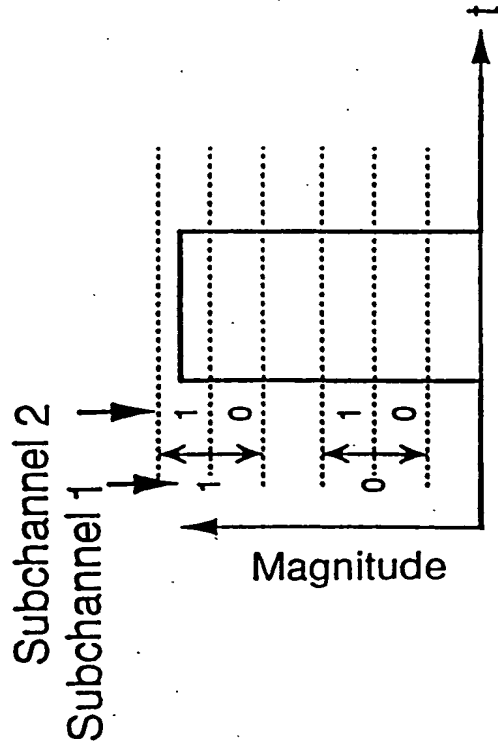


FIG. 60

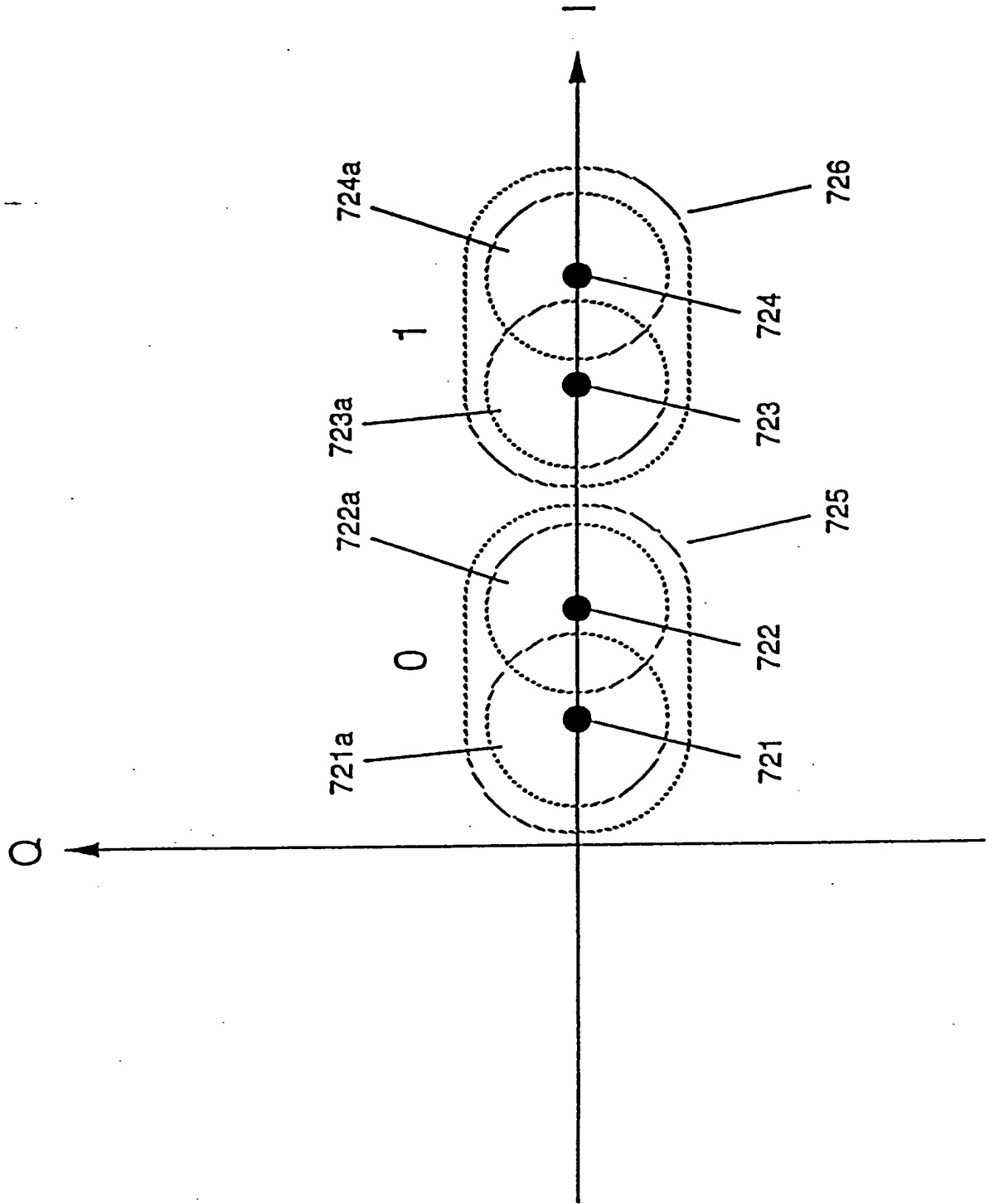


FIG. 61

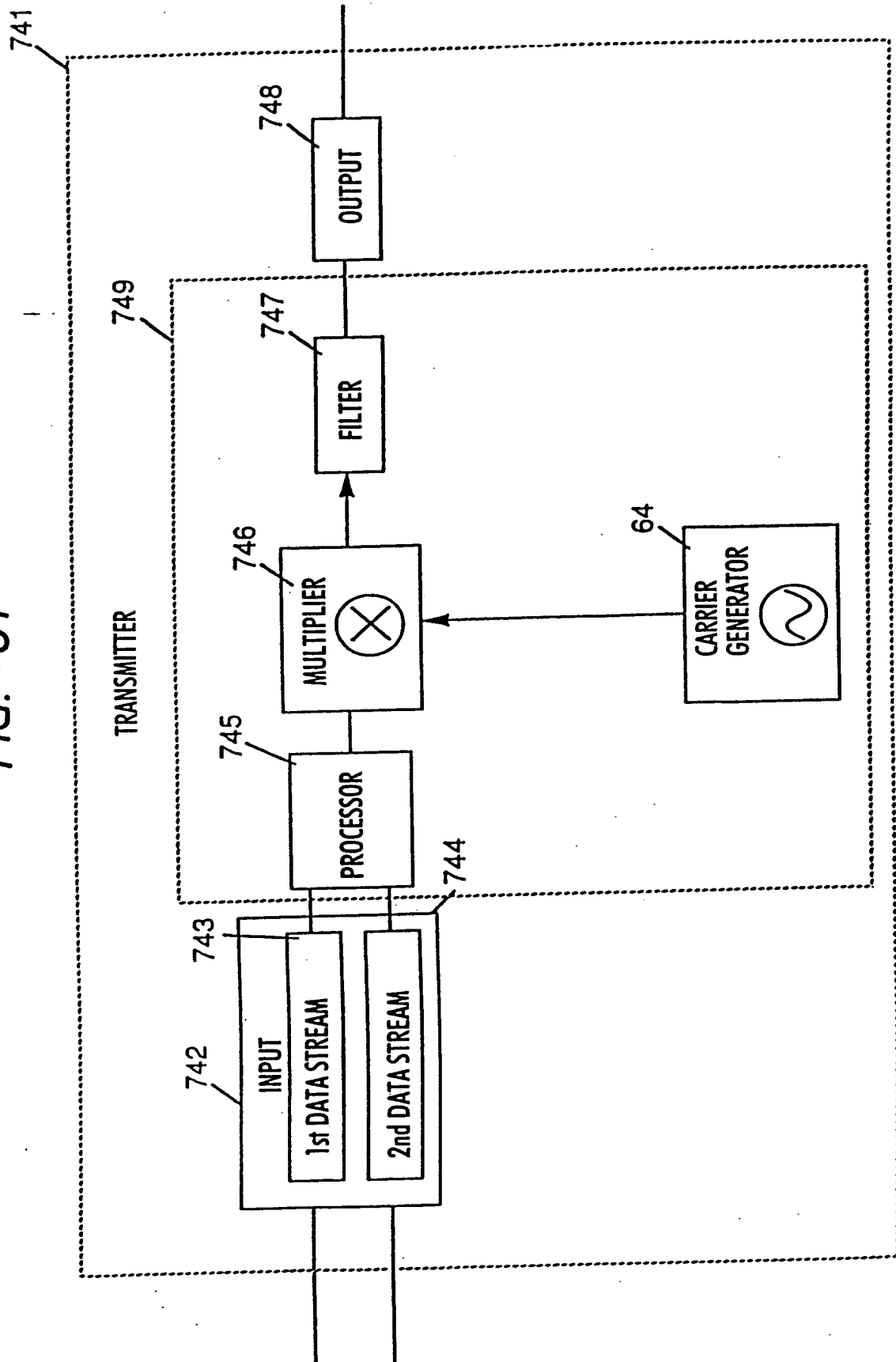


FIG. 62(a)

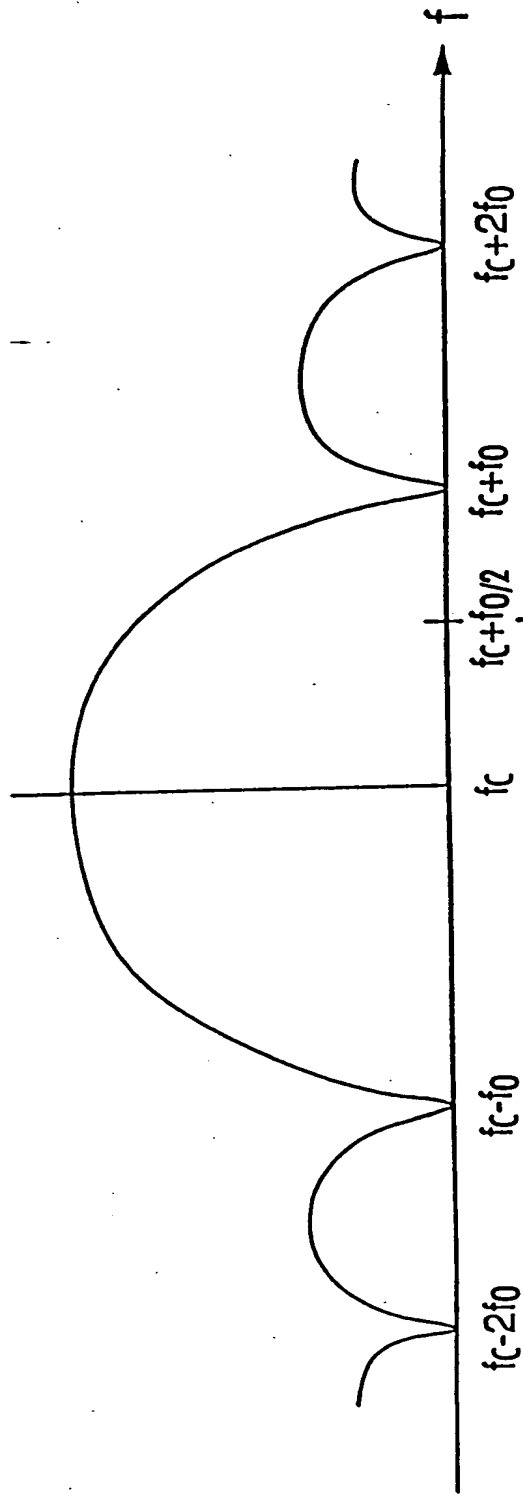


FIG. 62(b)

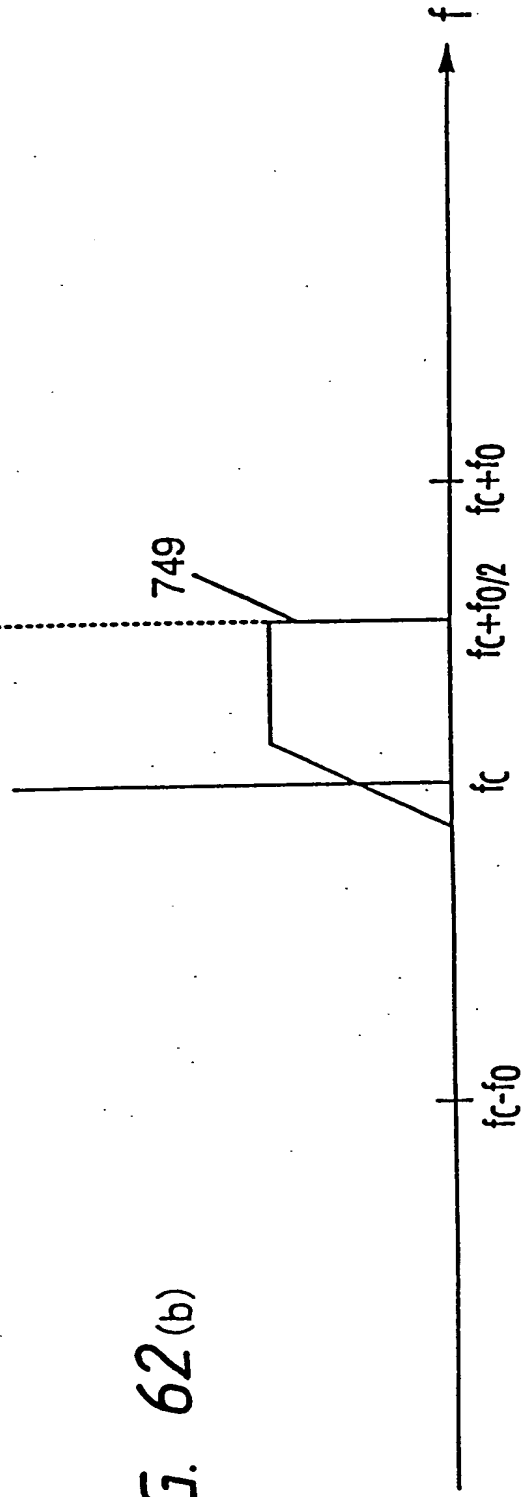


FIG. 63

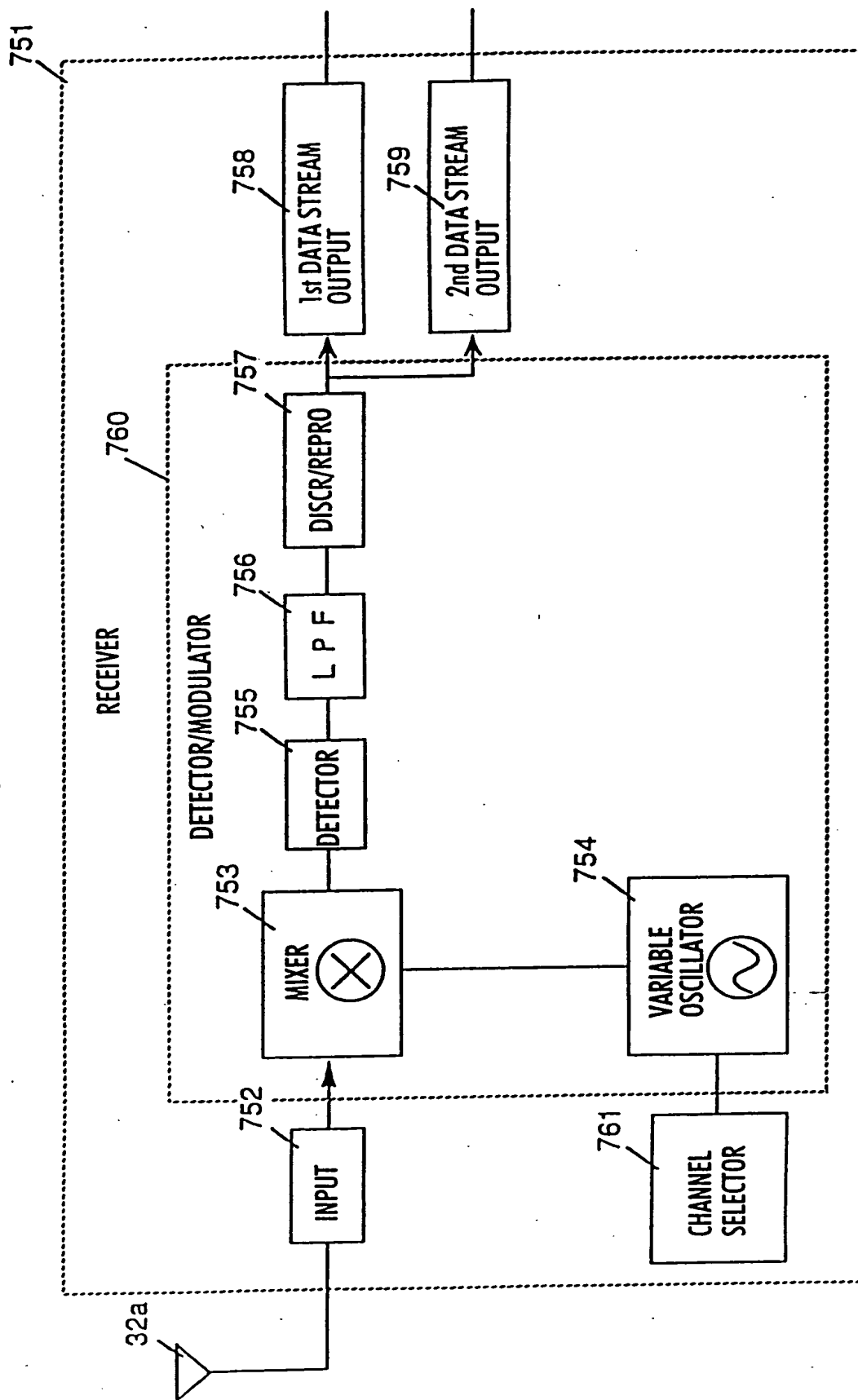


FIG. 64

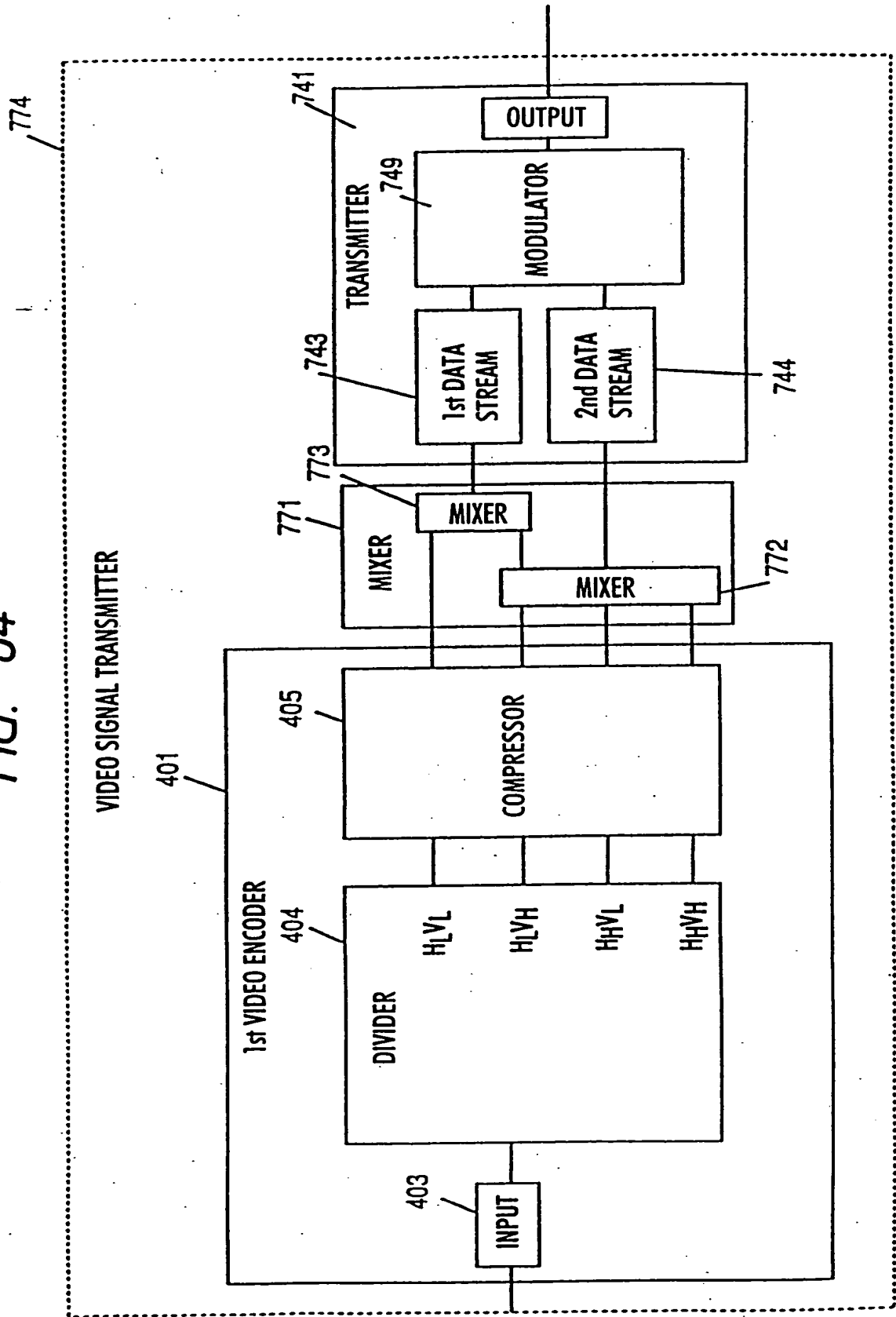




FIG. 65

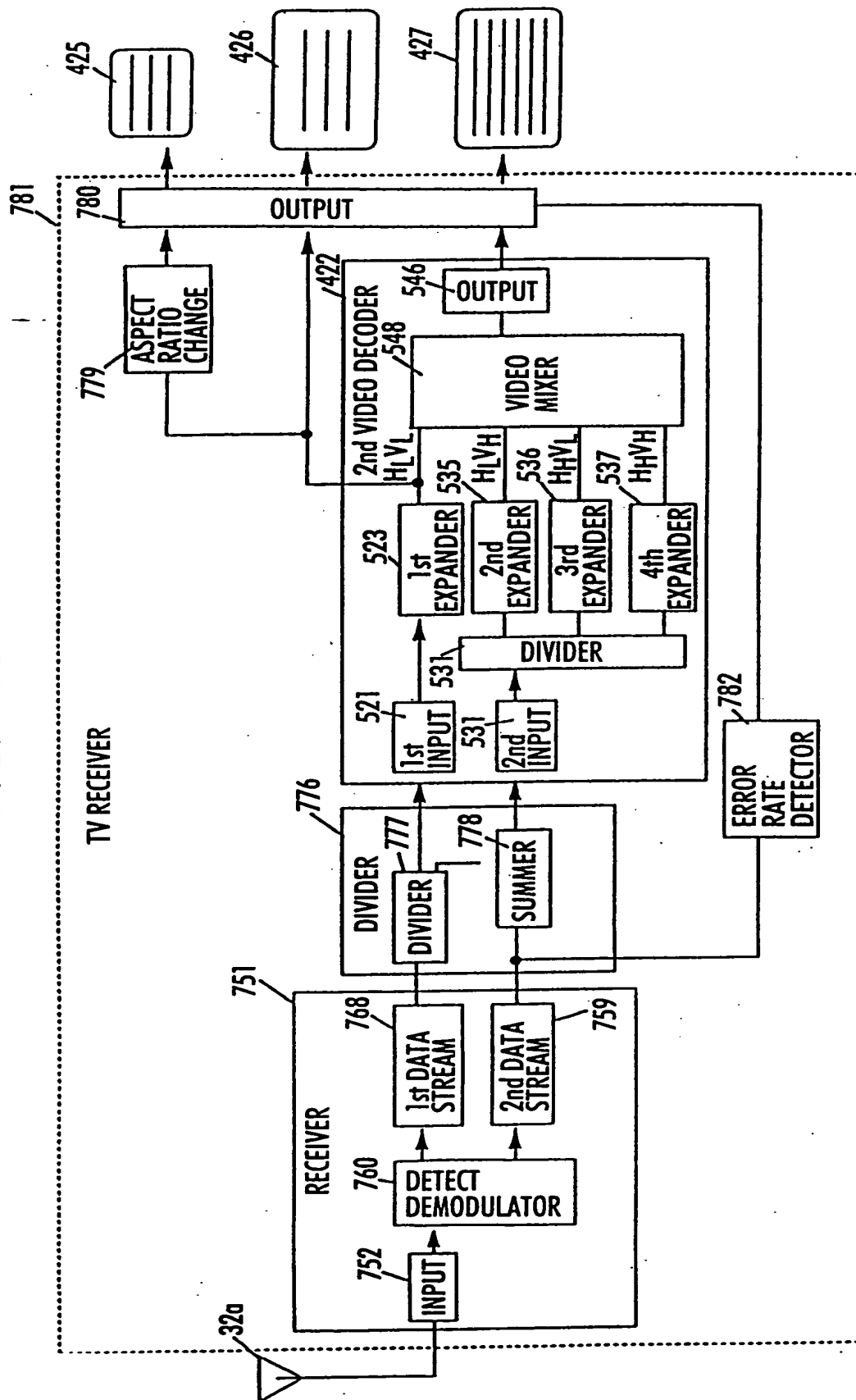


FIG. 66

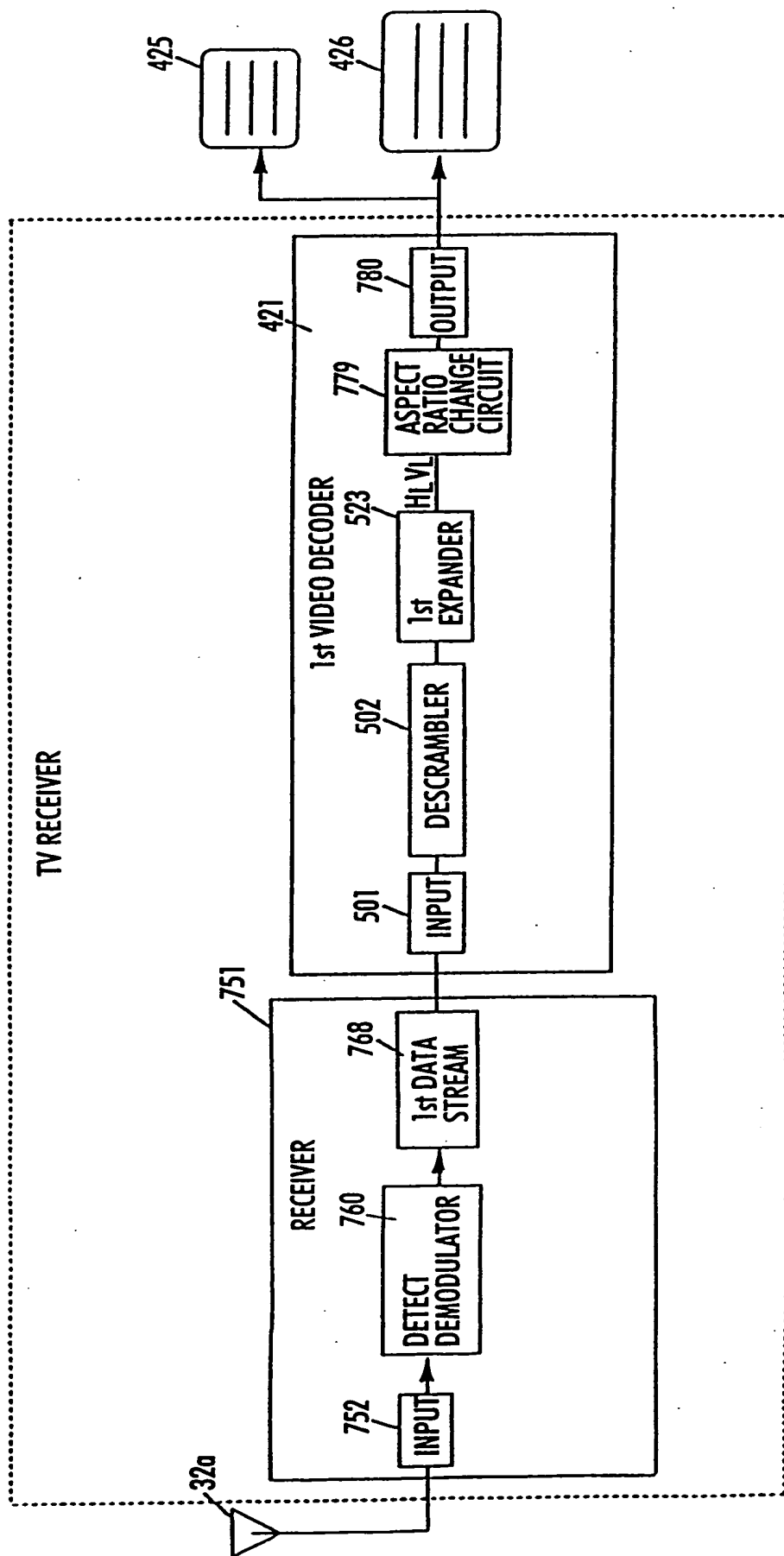
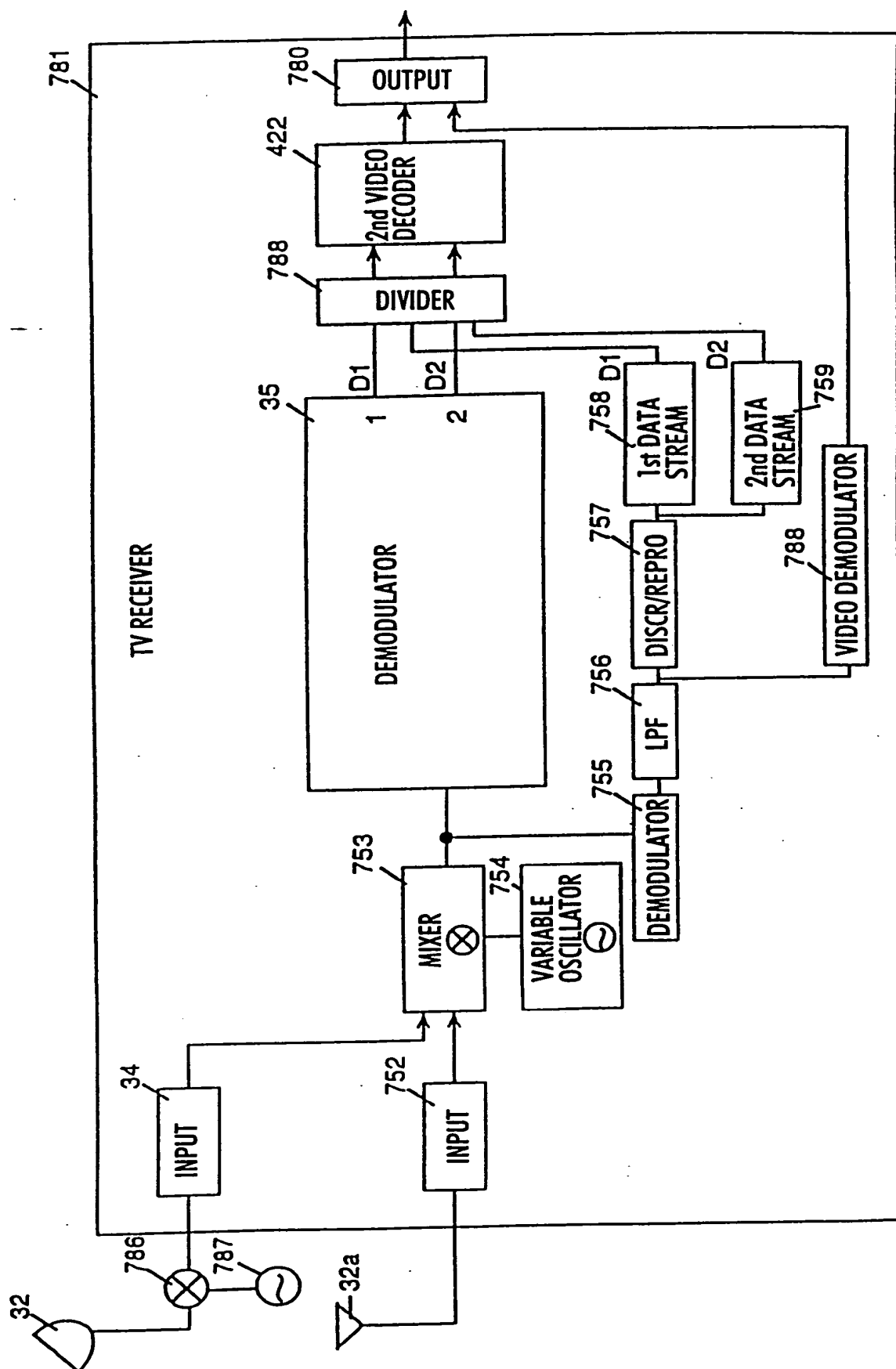


FIG. 67



Q →

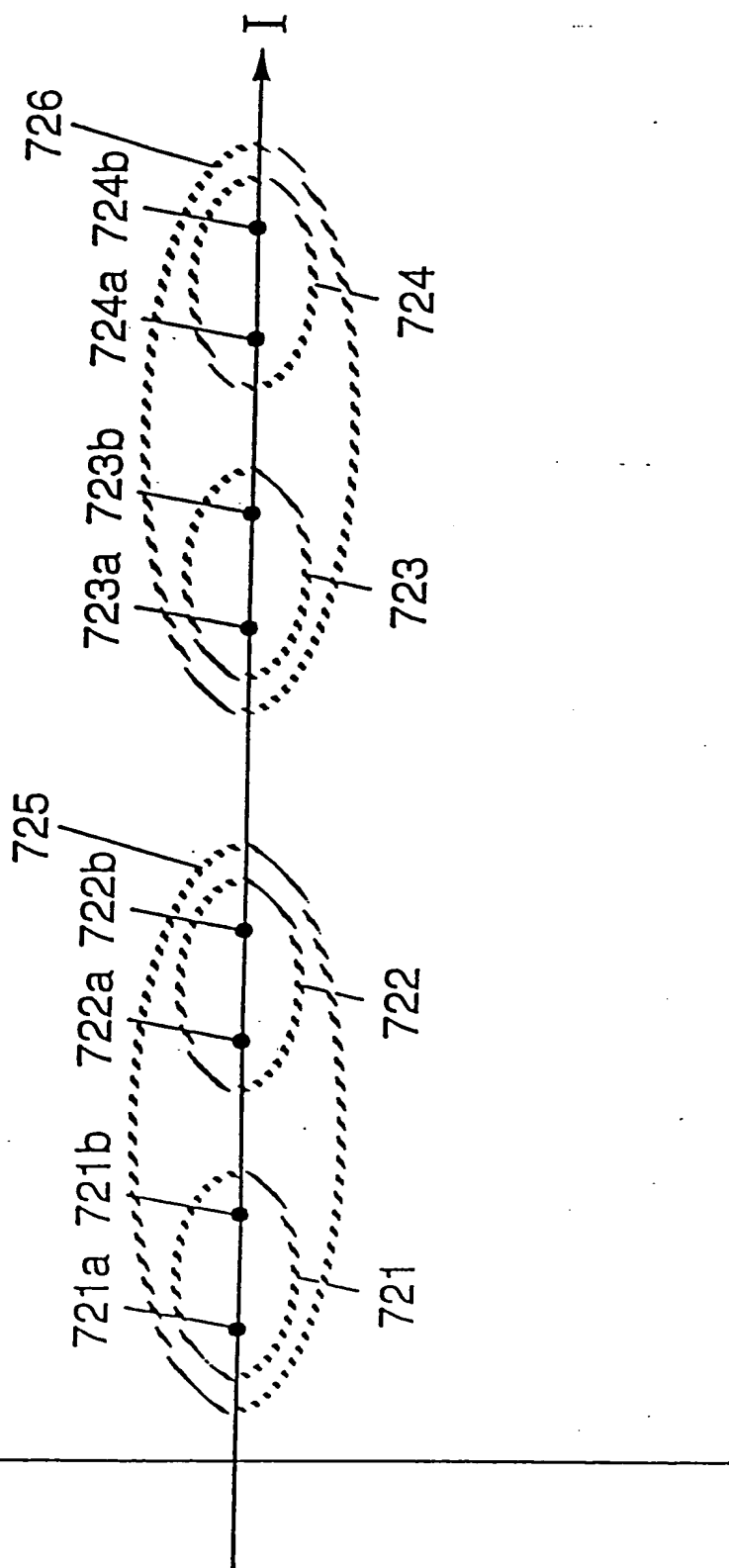


FIG. 69

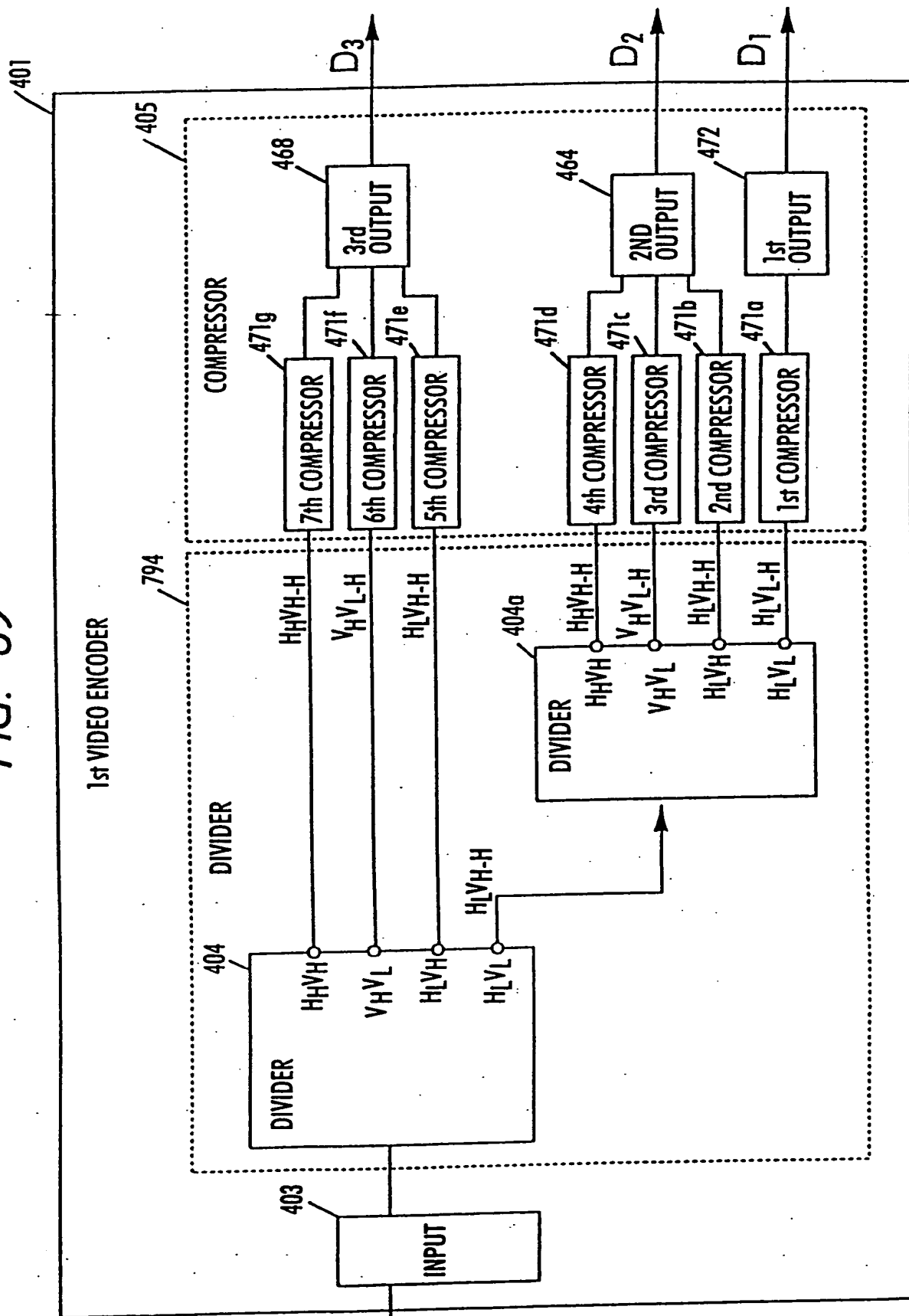


FIG. 70

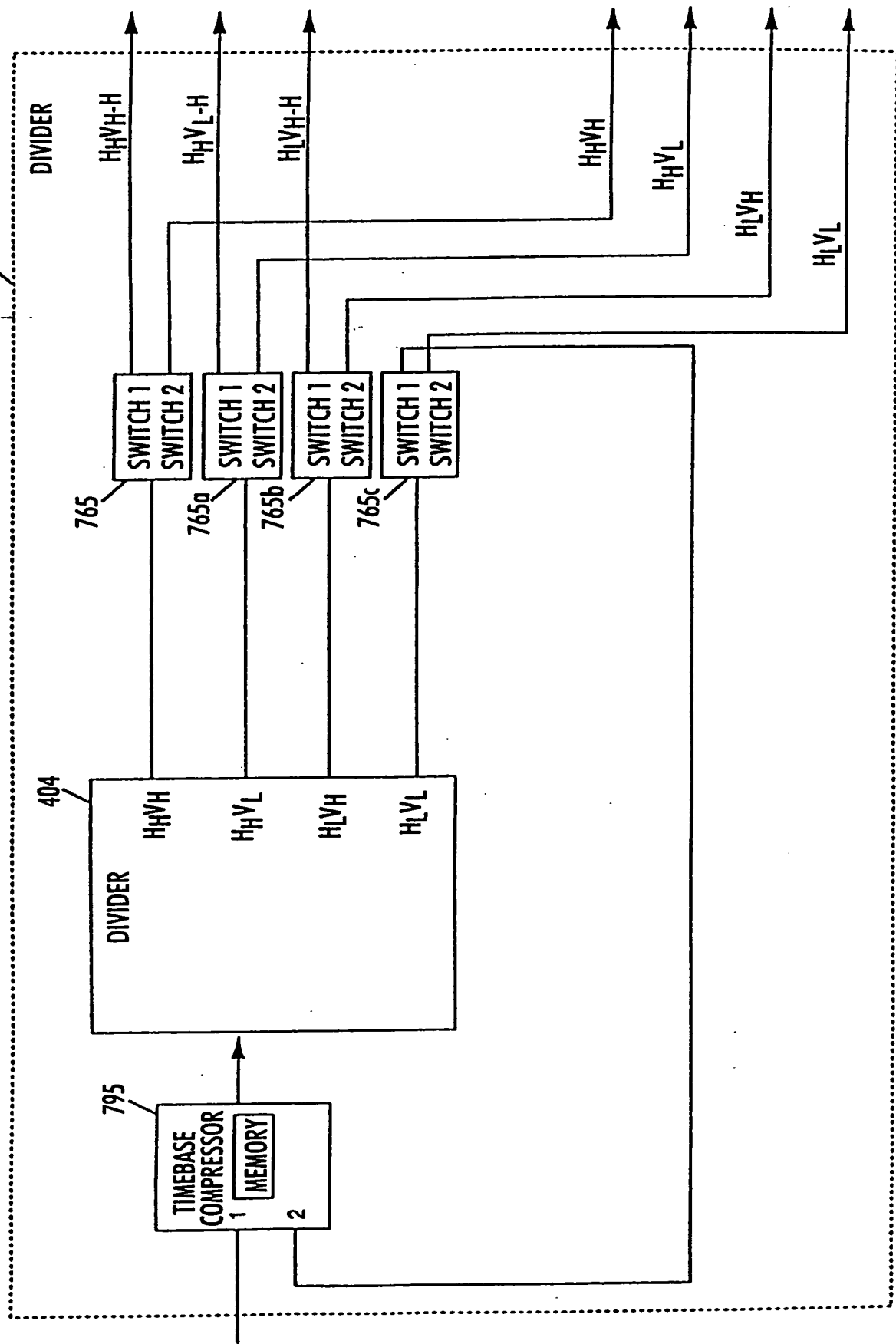


FIG. 71

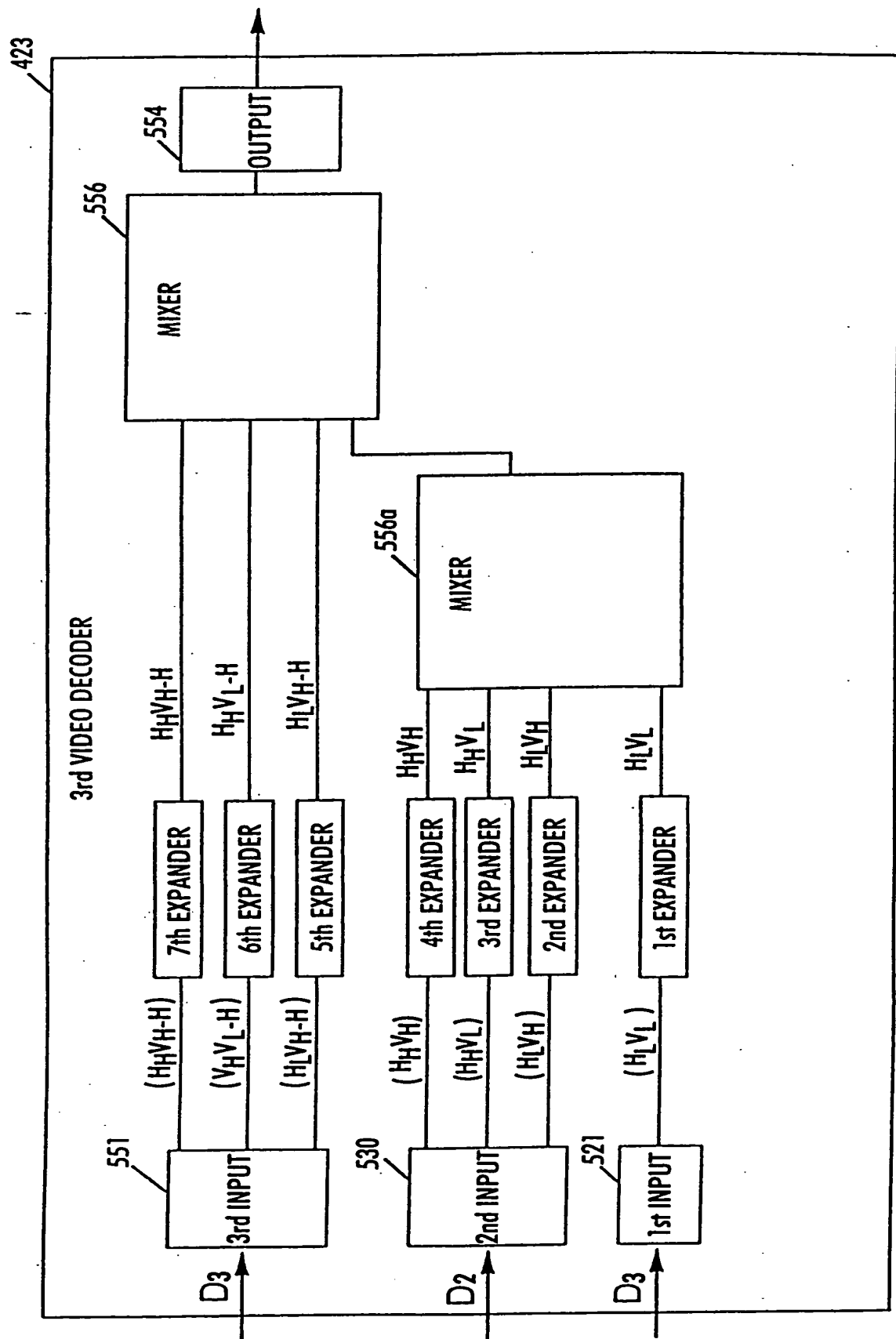


FIG. 72

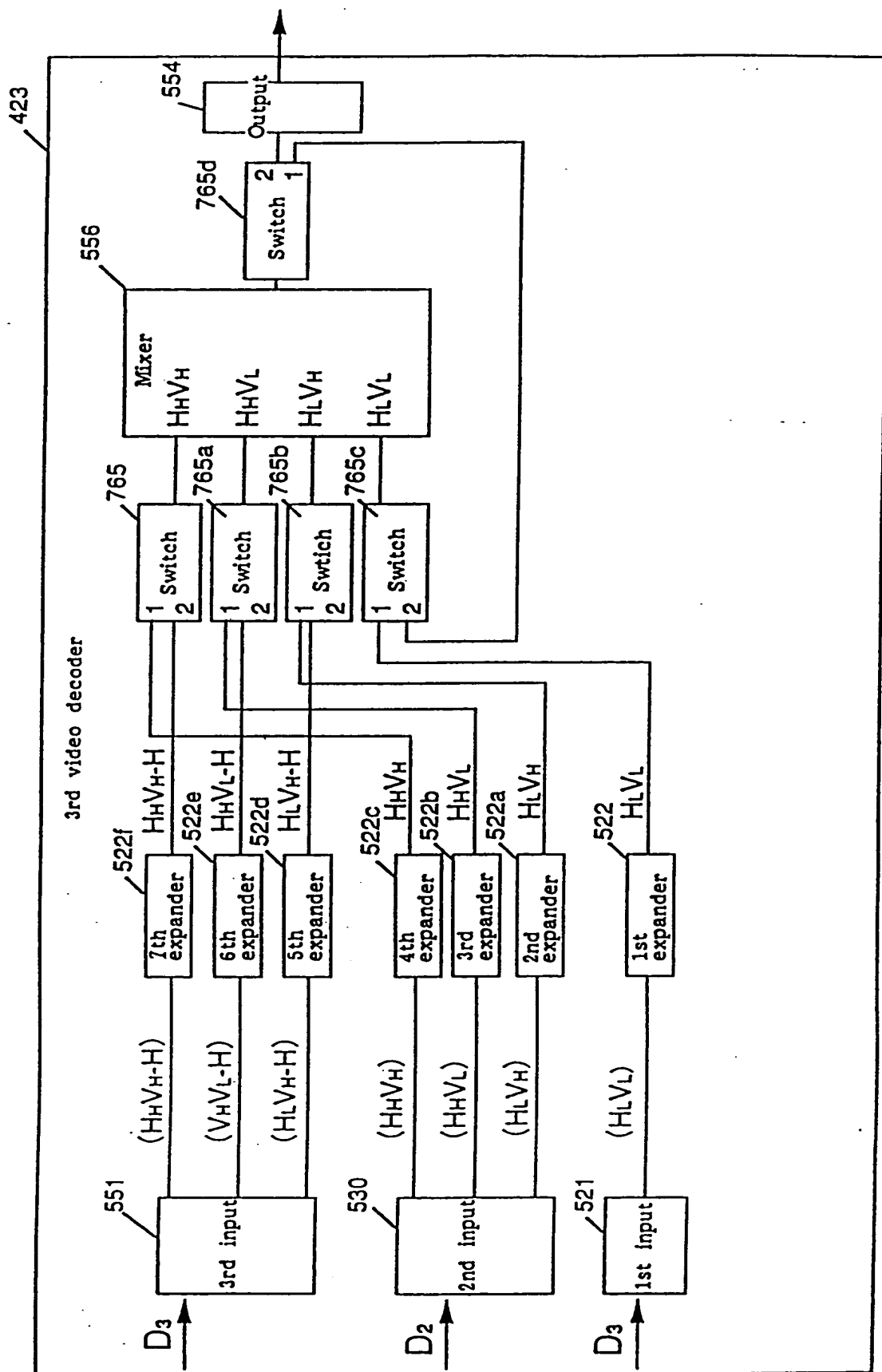




FIG. 73

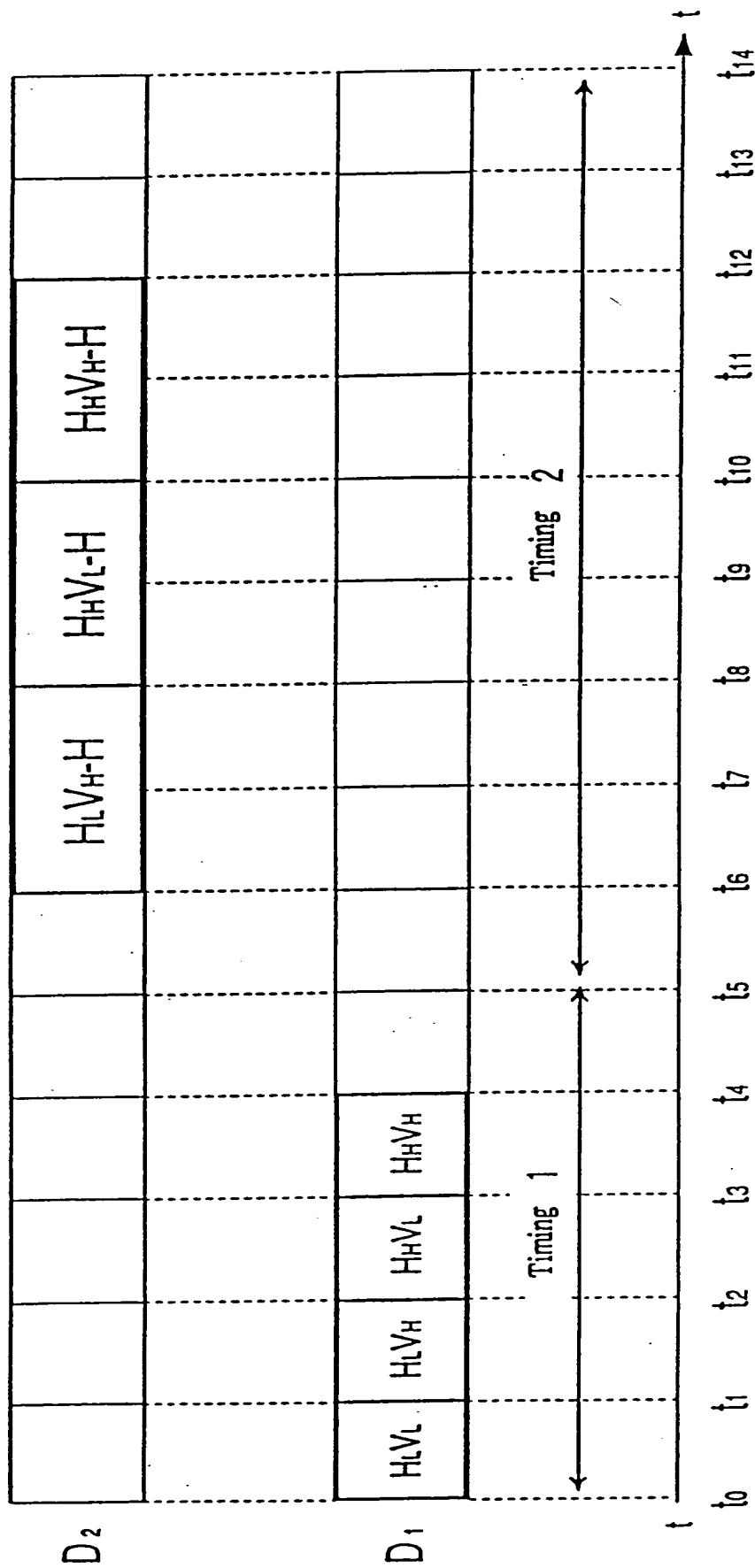


FIG. 74 (a)

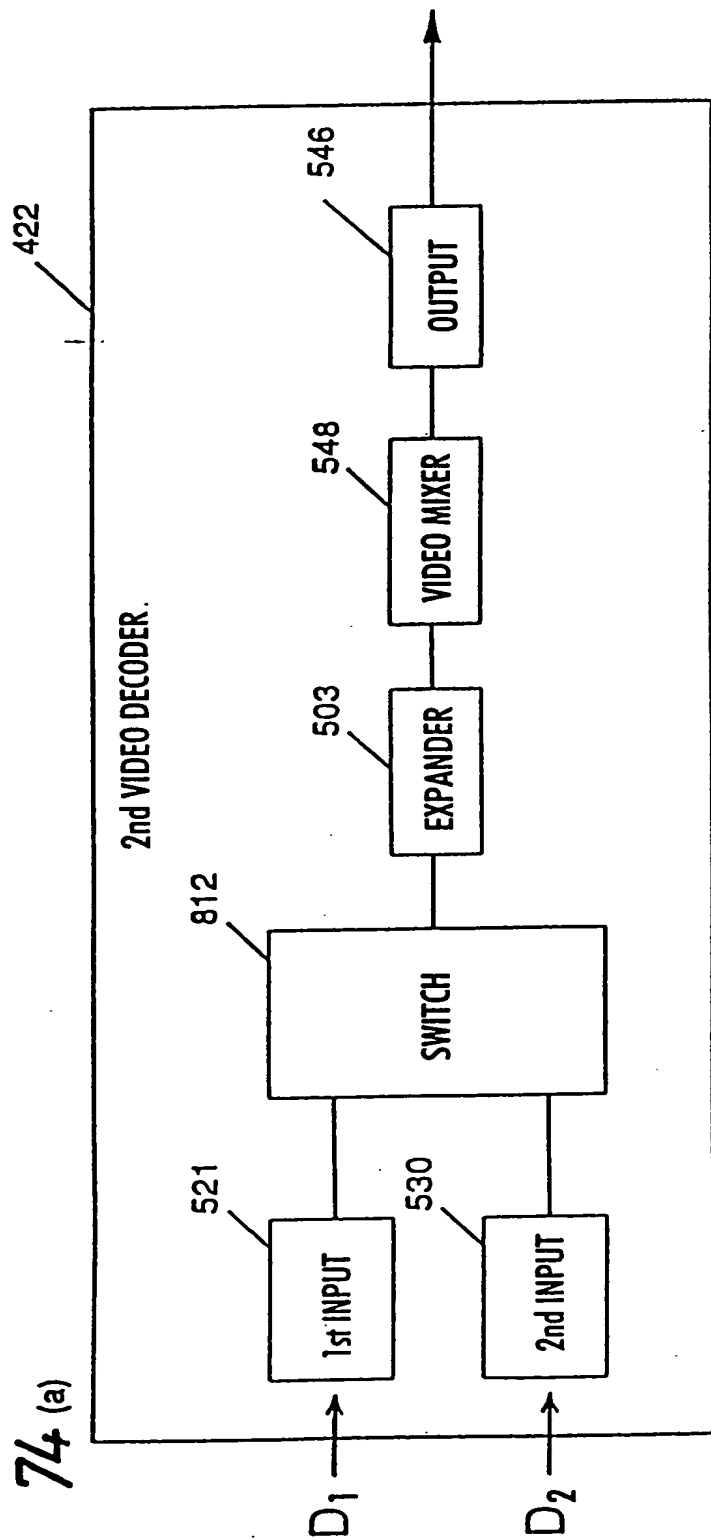


FIG. 74 (b)

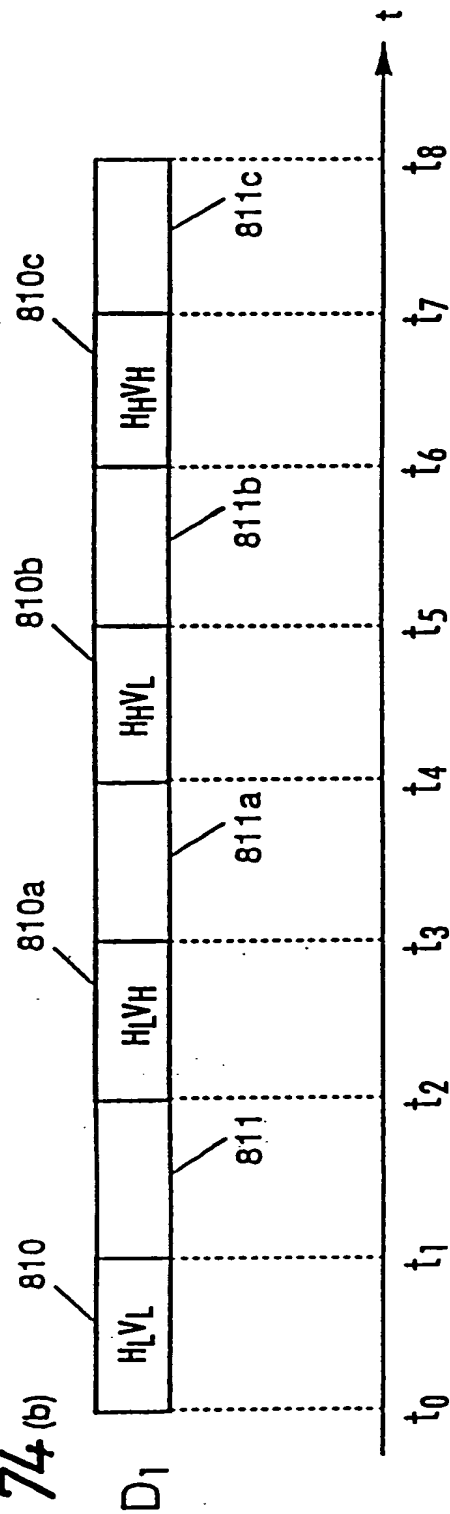


FIG. 75

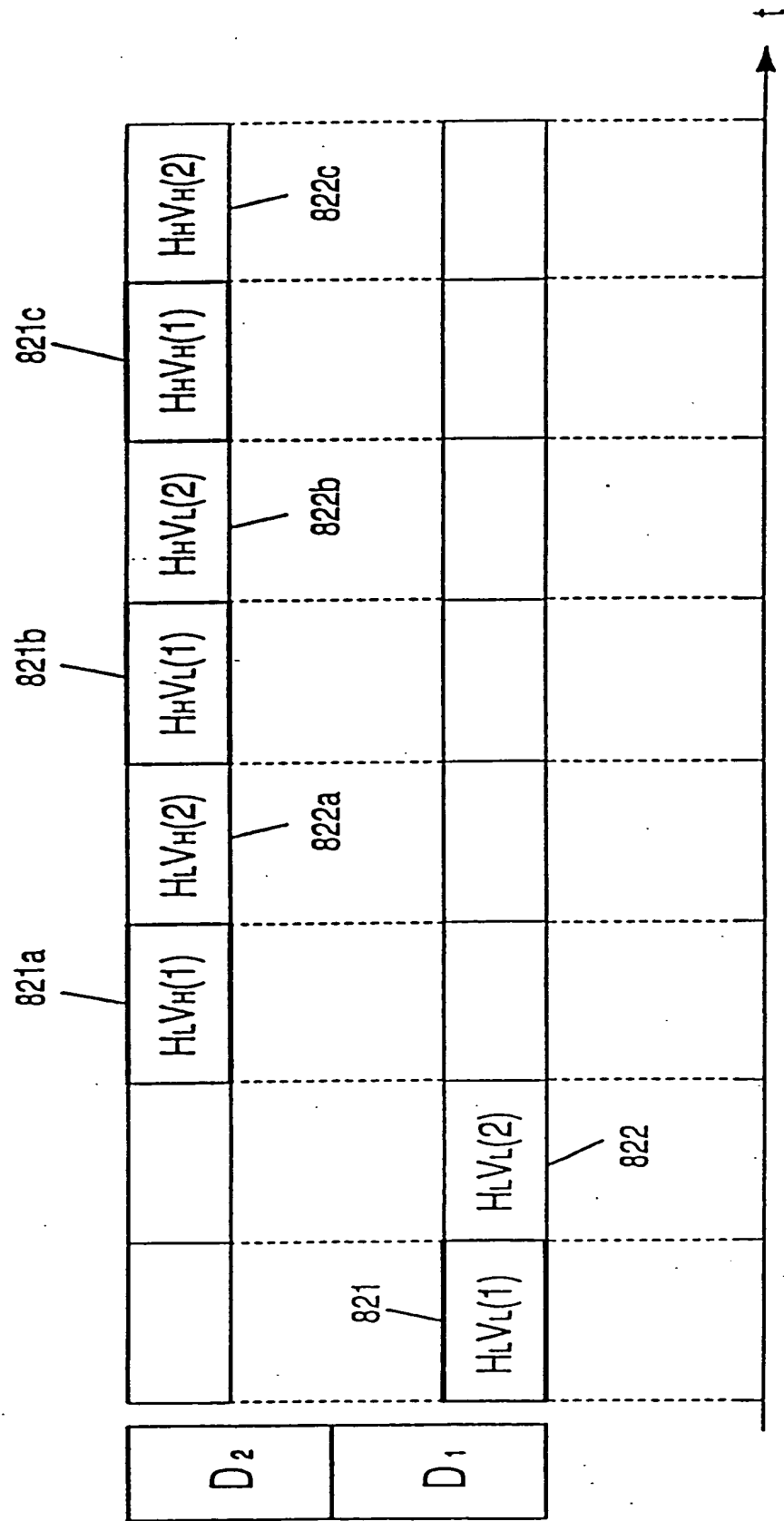


FIG. 76

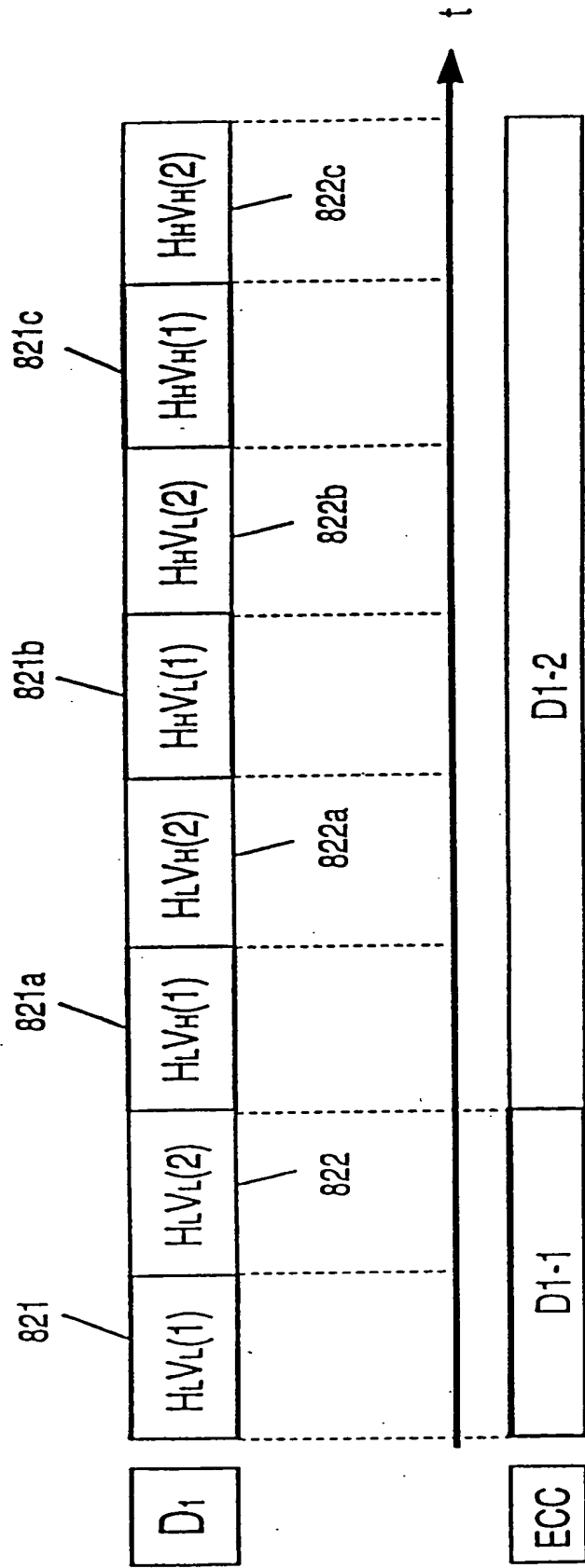


FIG. 77

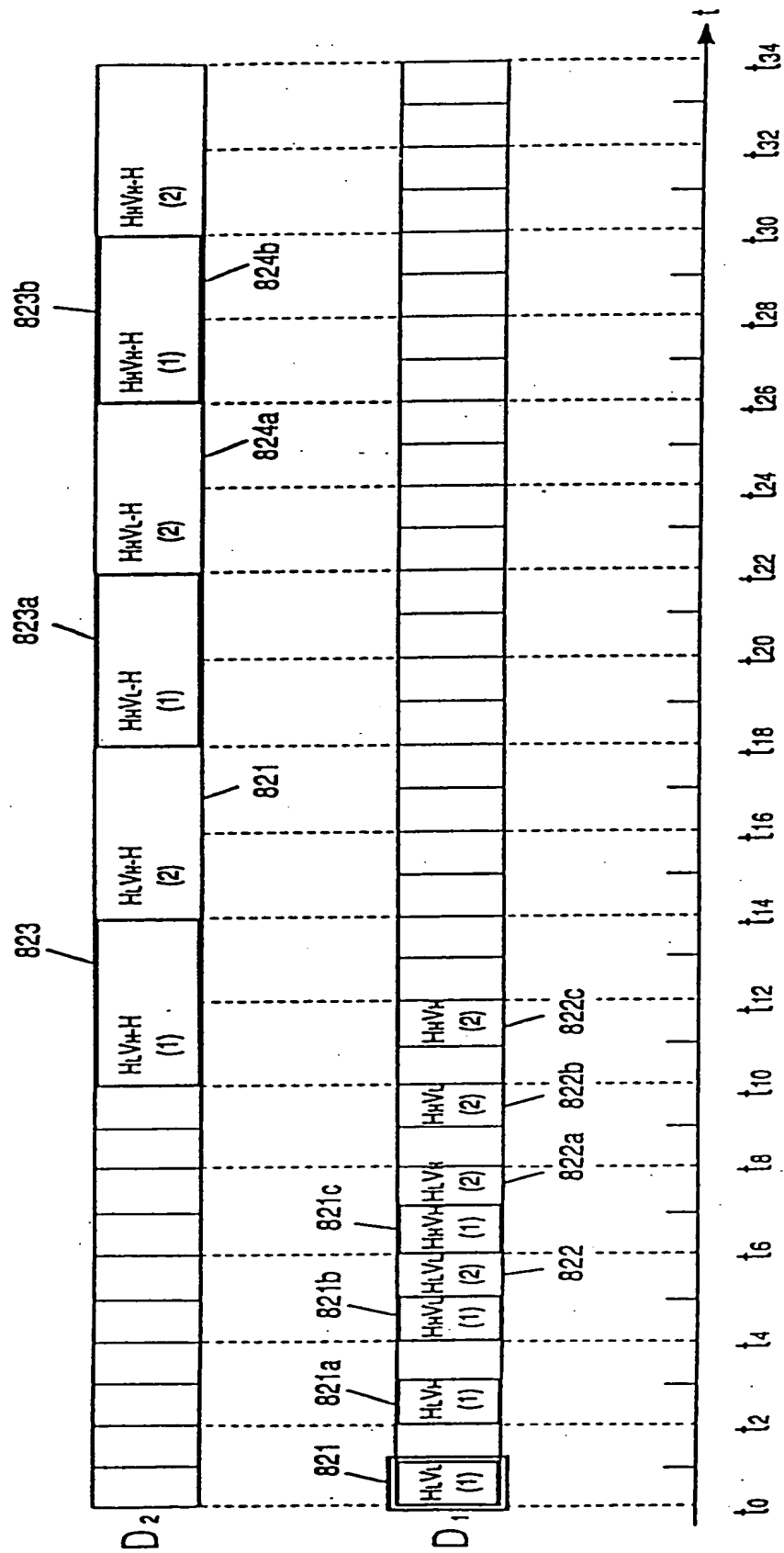


FIG. 78

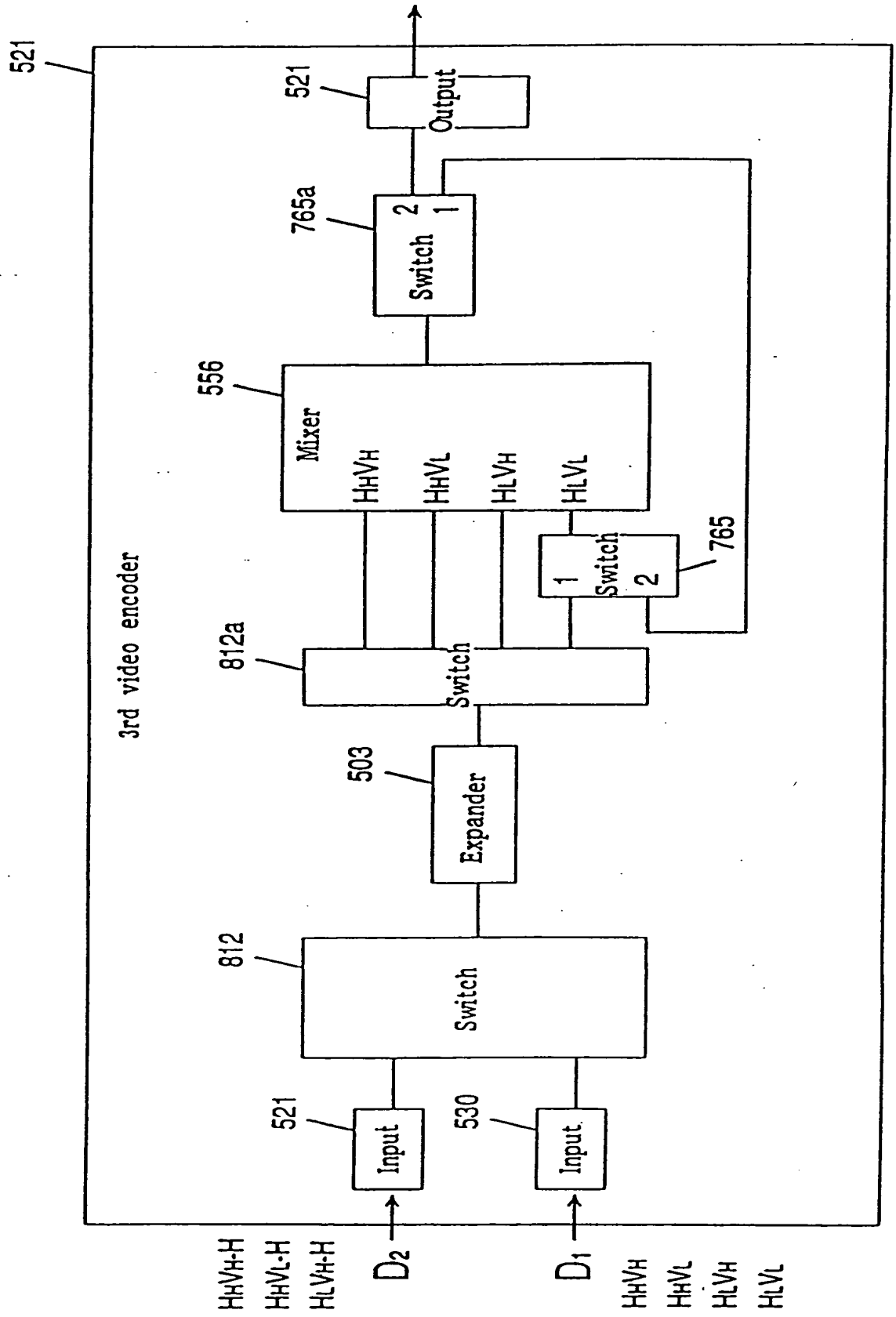


FIG. 79

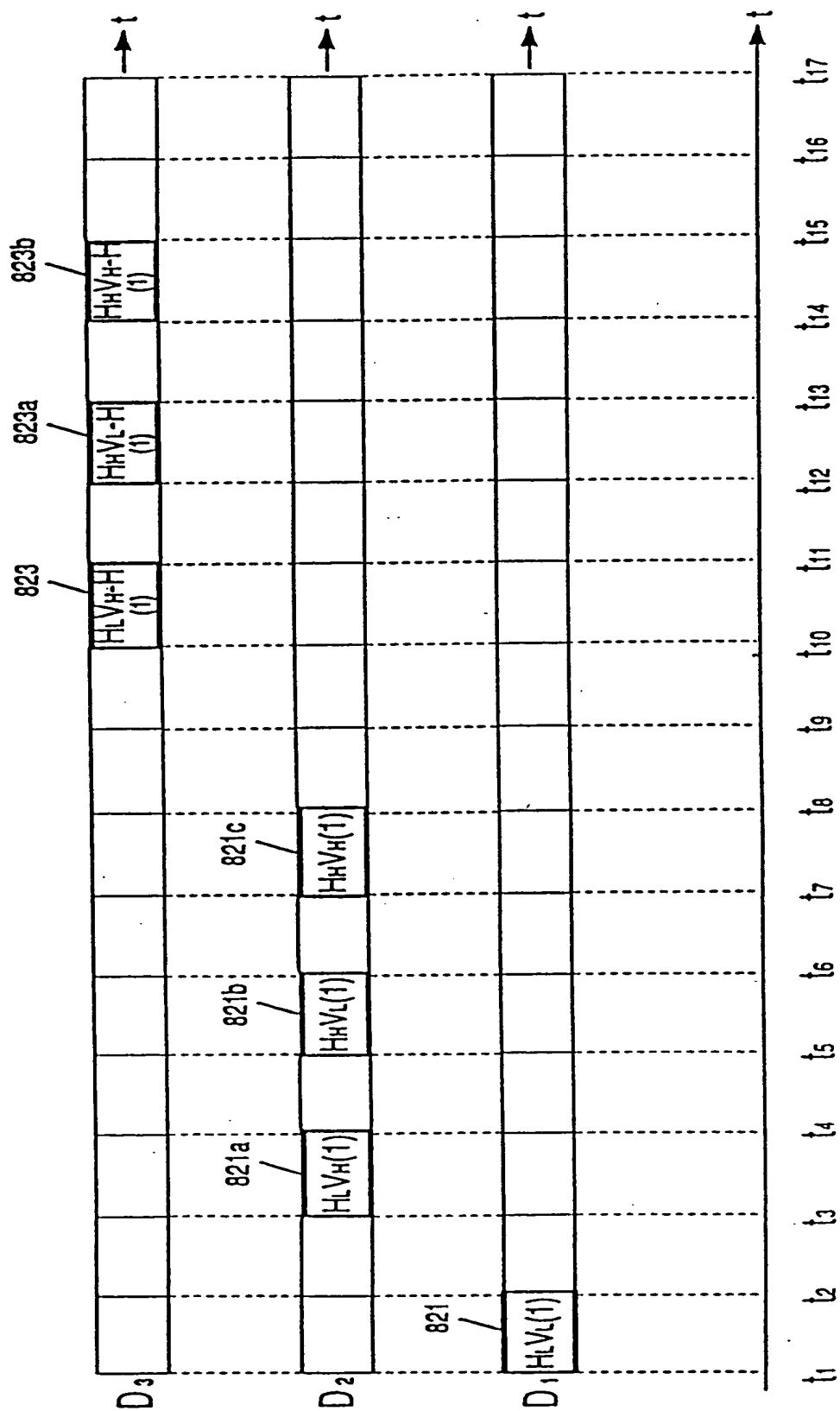


FIG. 80

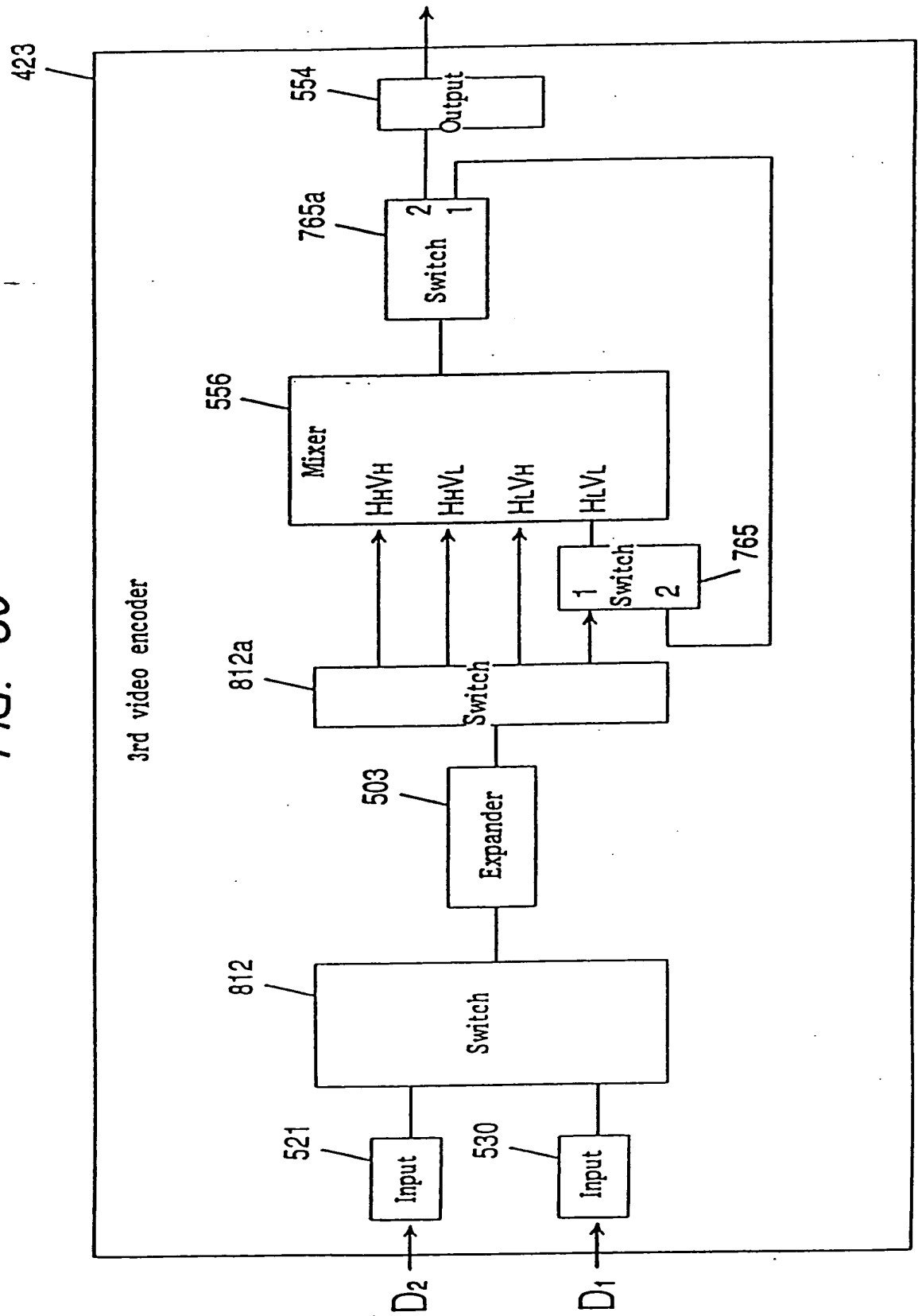




FIG. 81

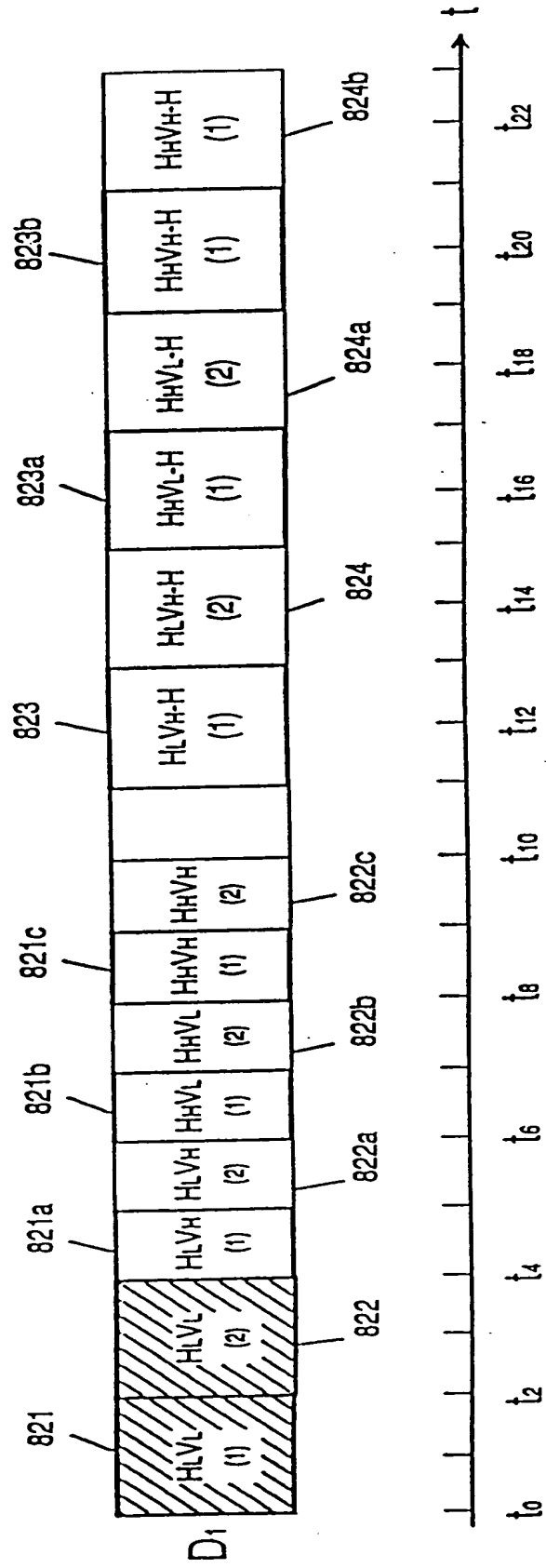


FIG. 82

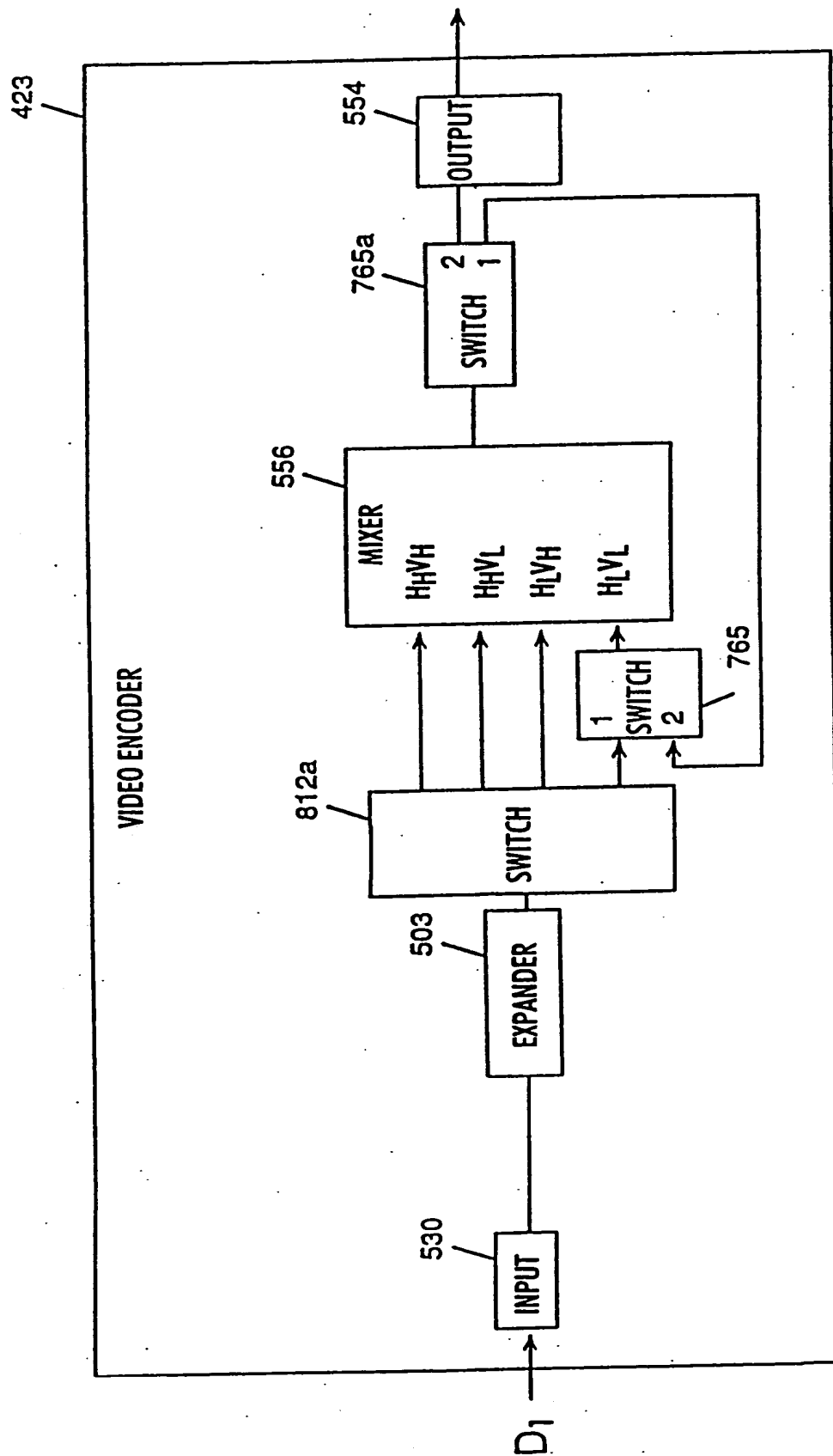


FIG. 83

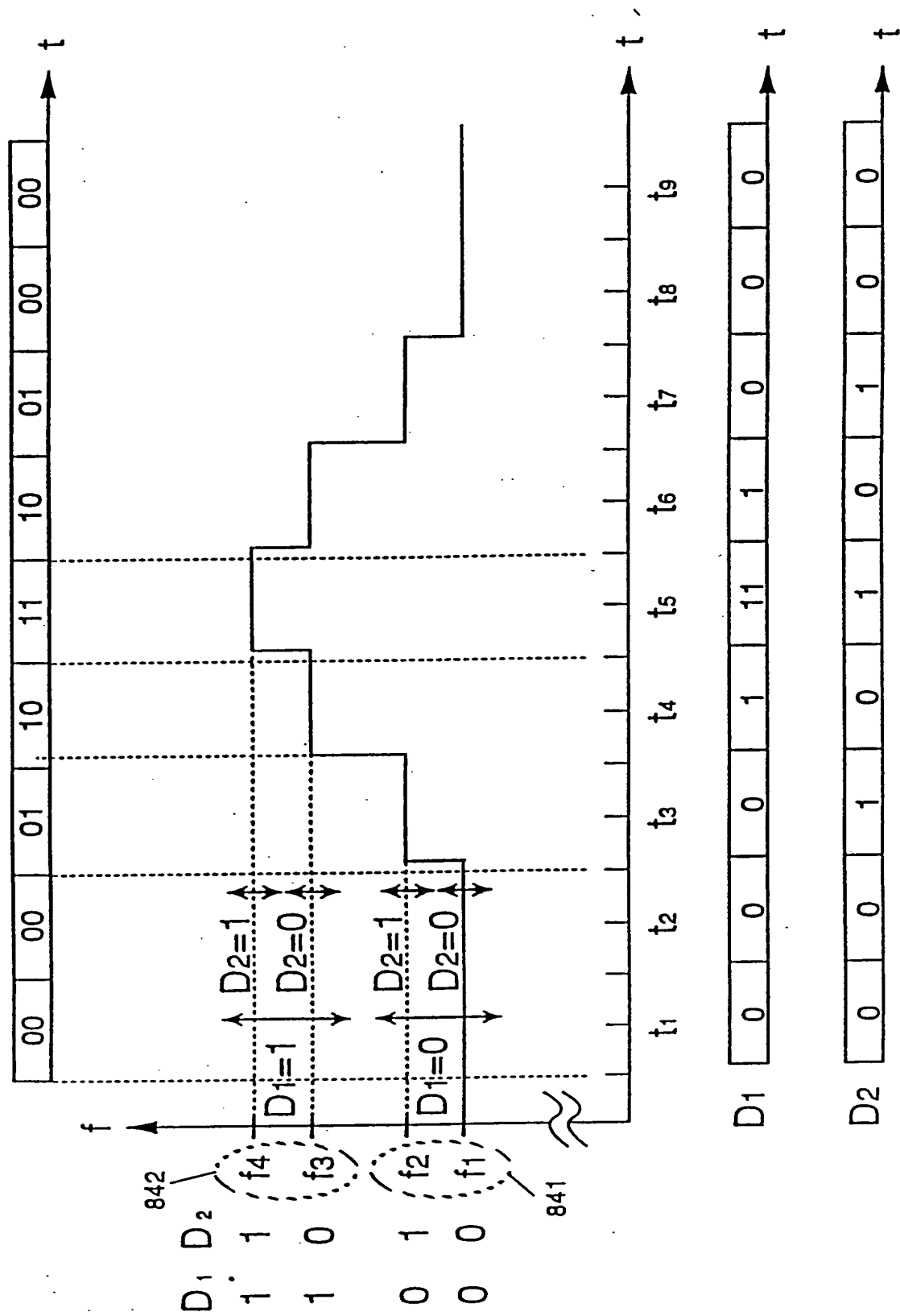


FIG. 84

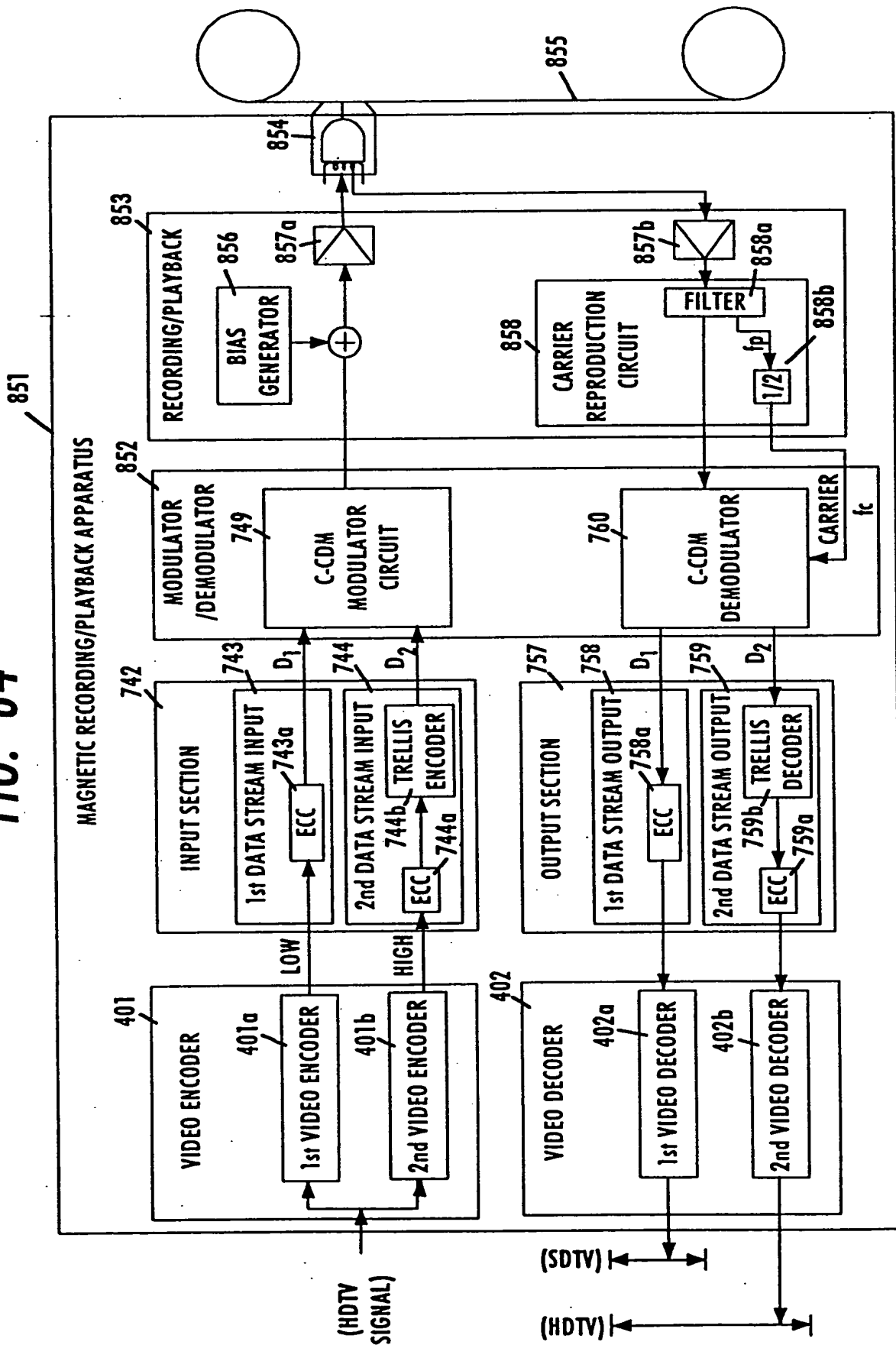


FIG. 85

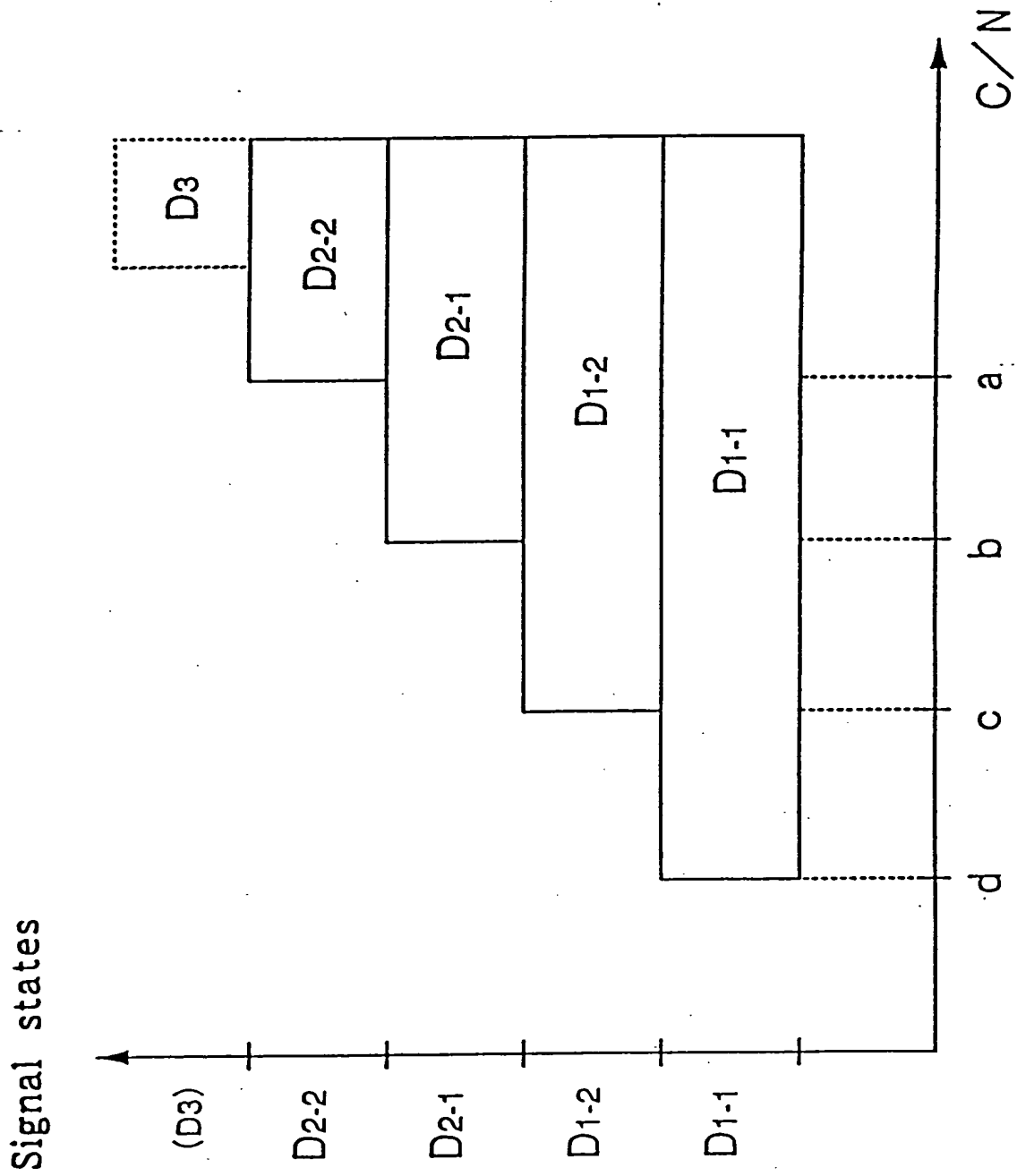


FIG. 86

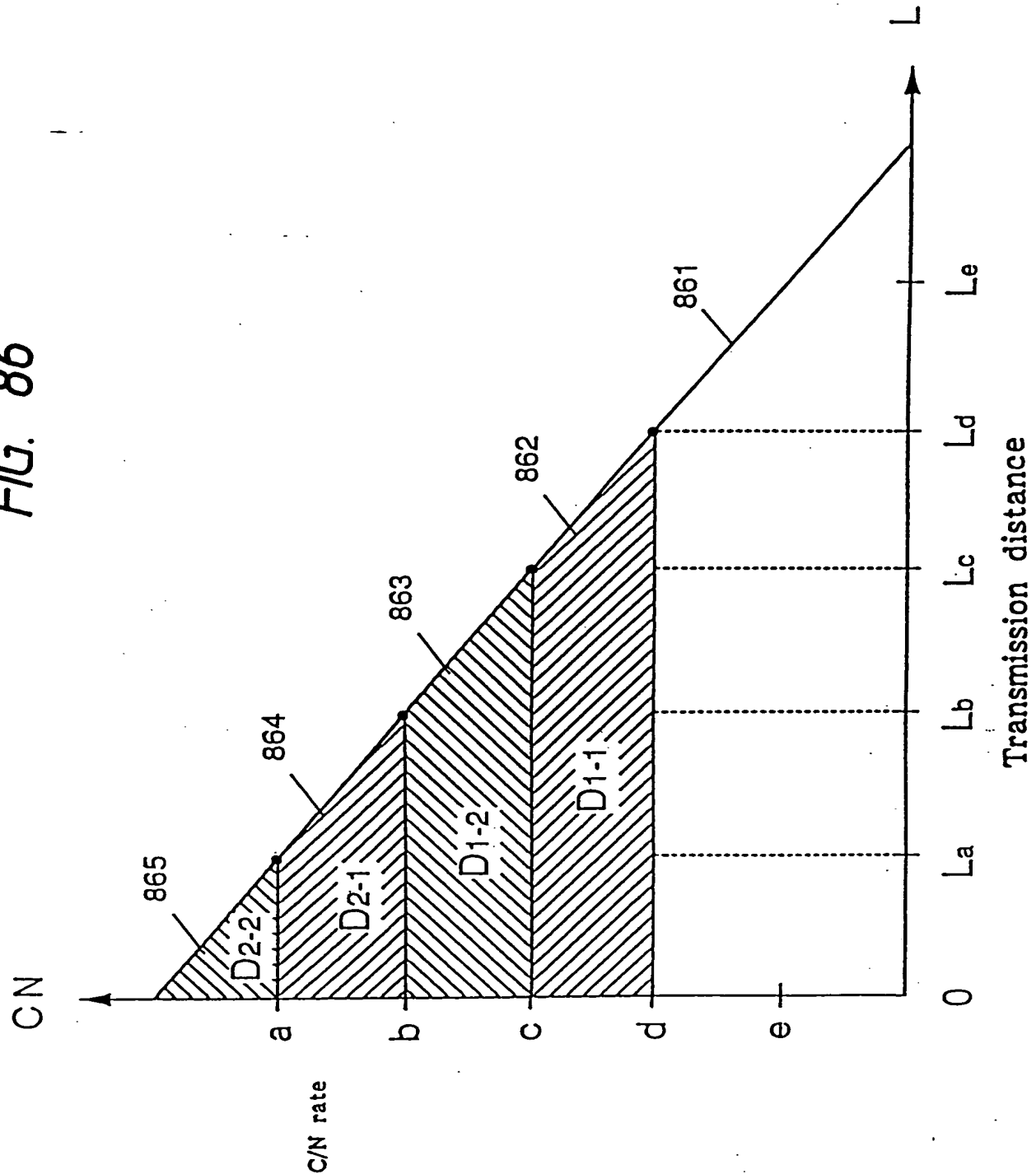


FIG. 87

TRANSMITTER

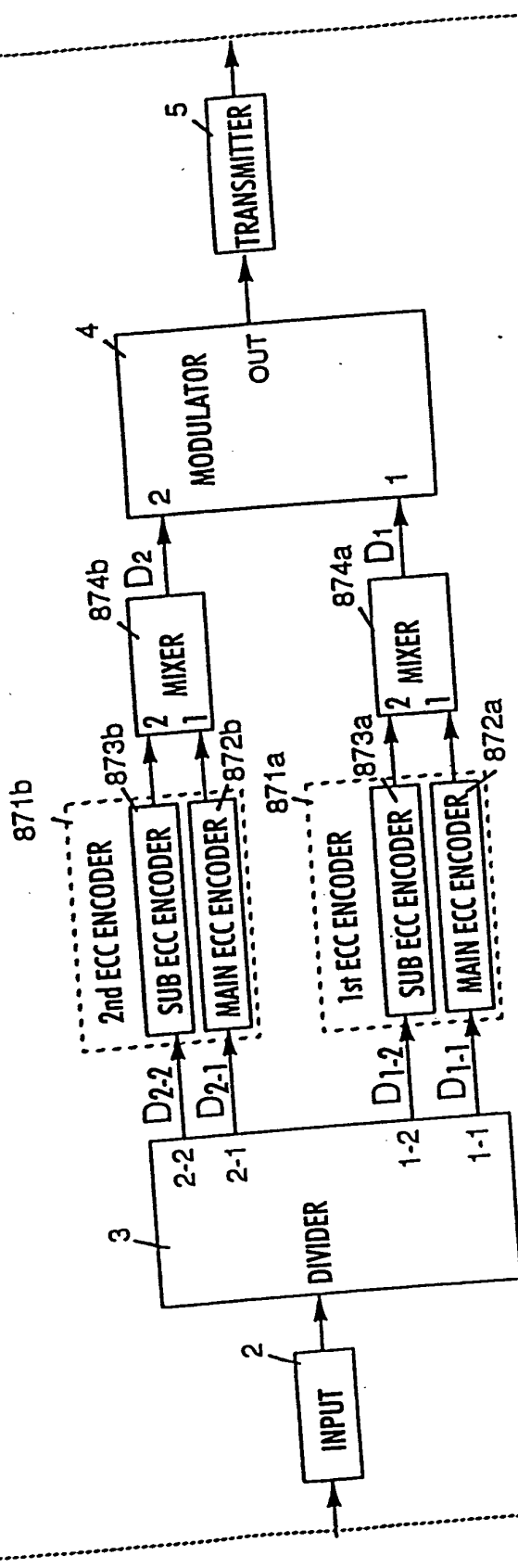


FIG. 88

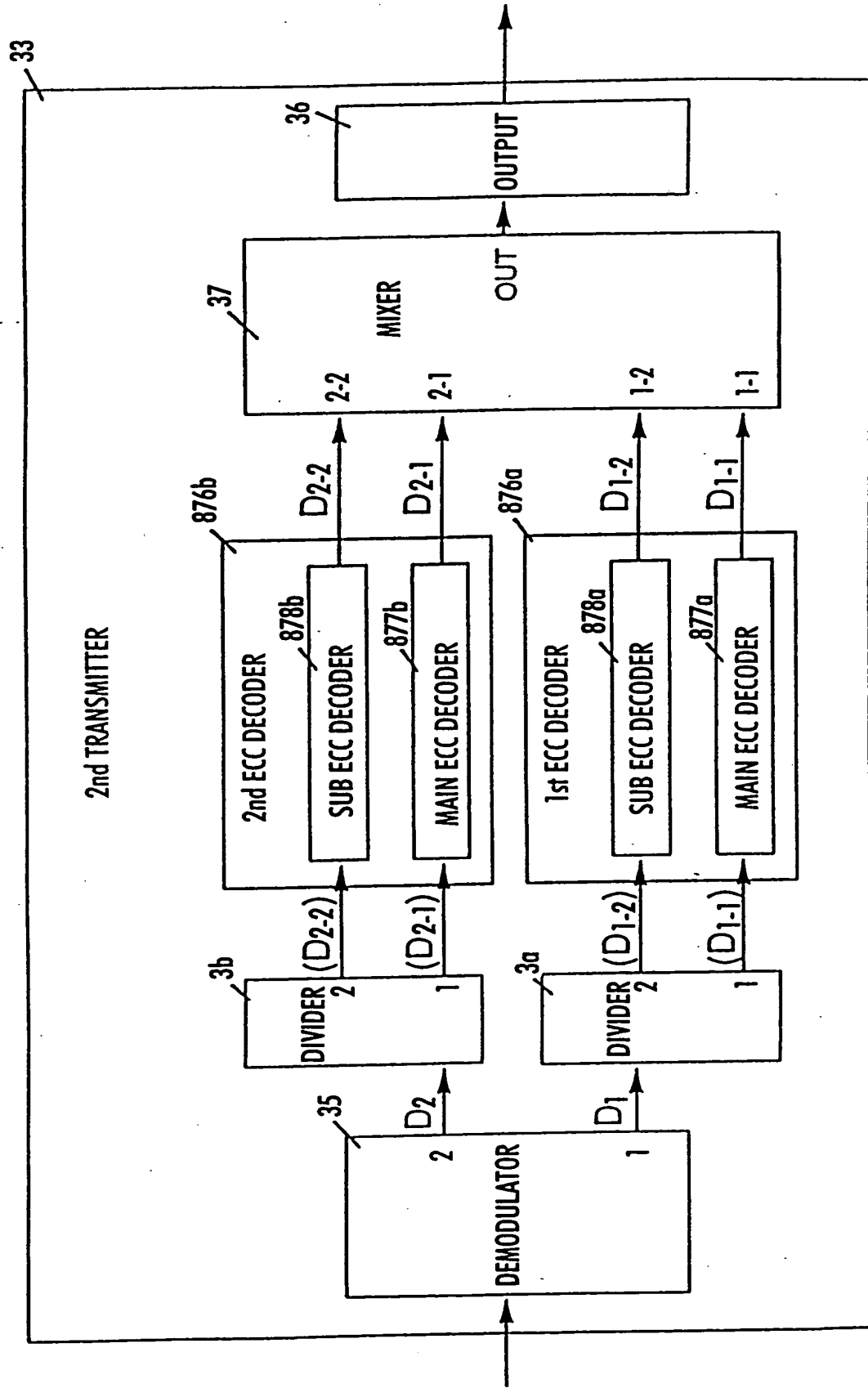




FIG. 89

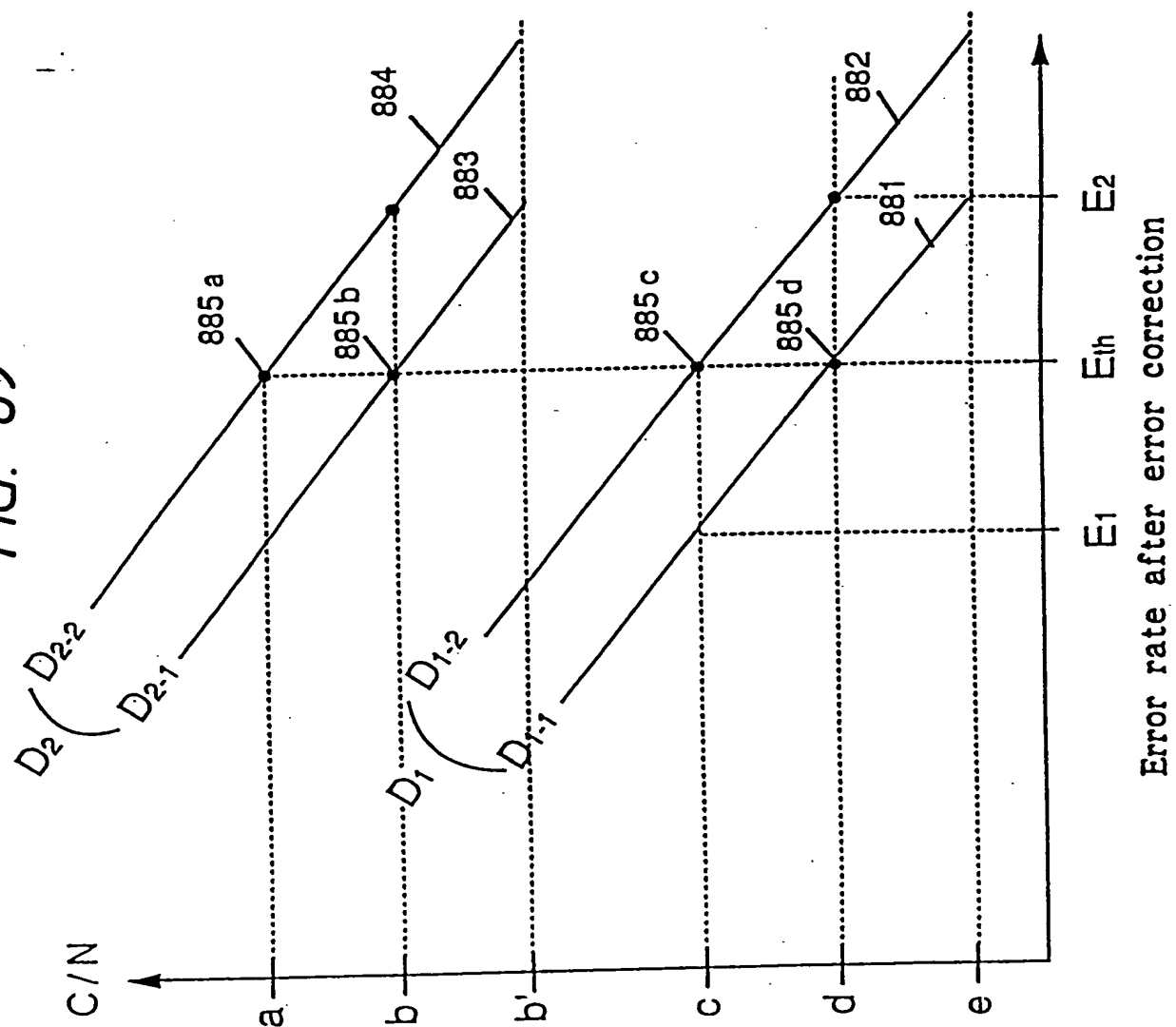


FIG. 90

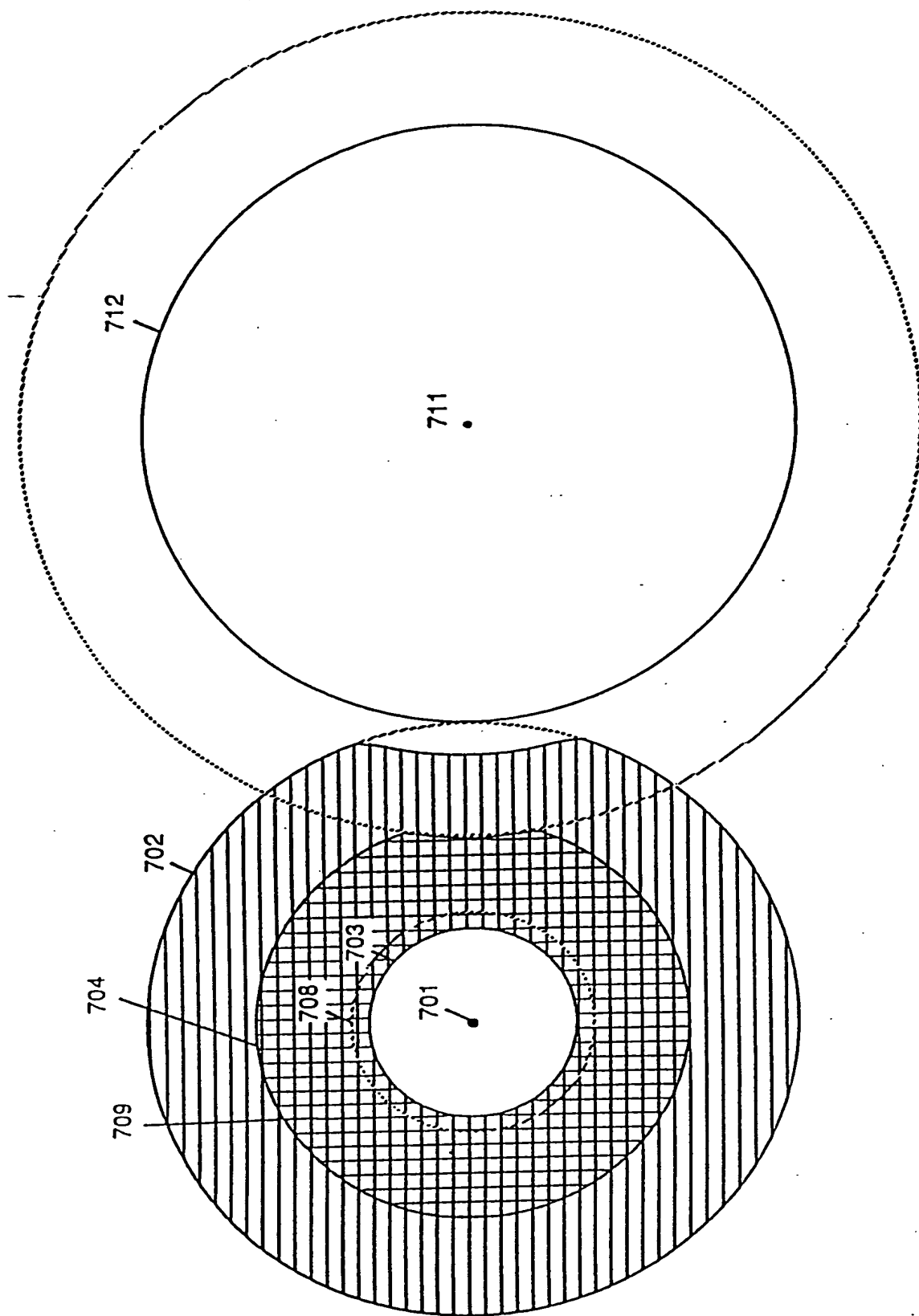


FIG. 91

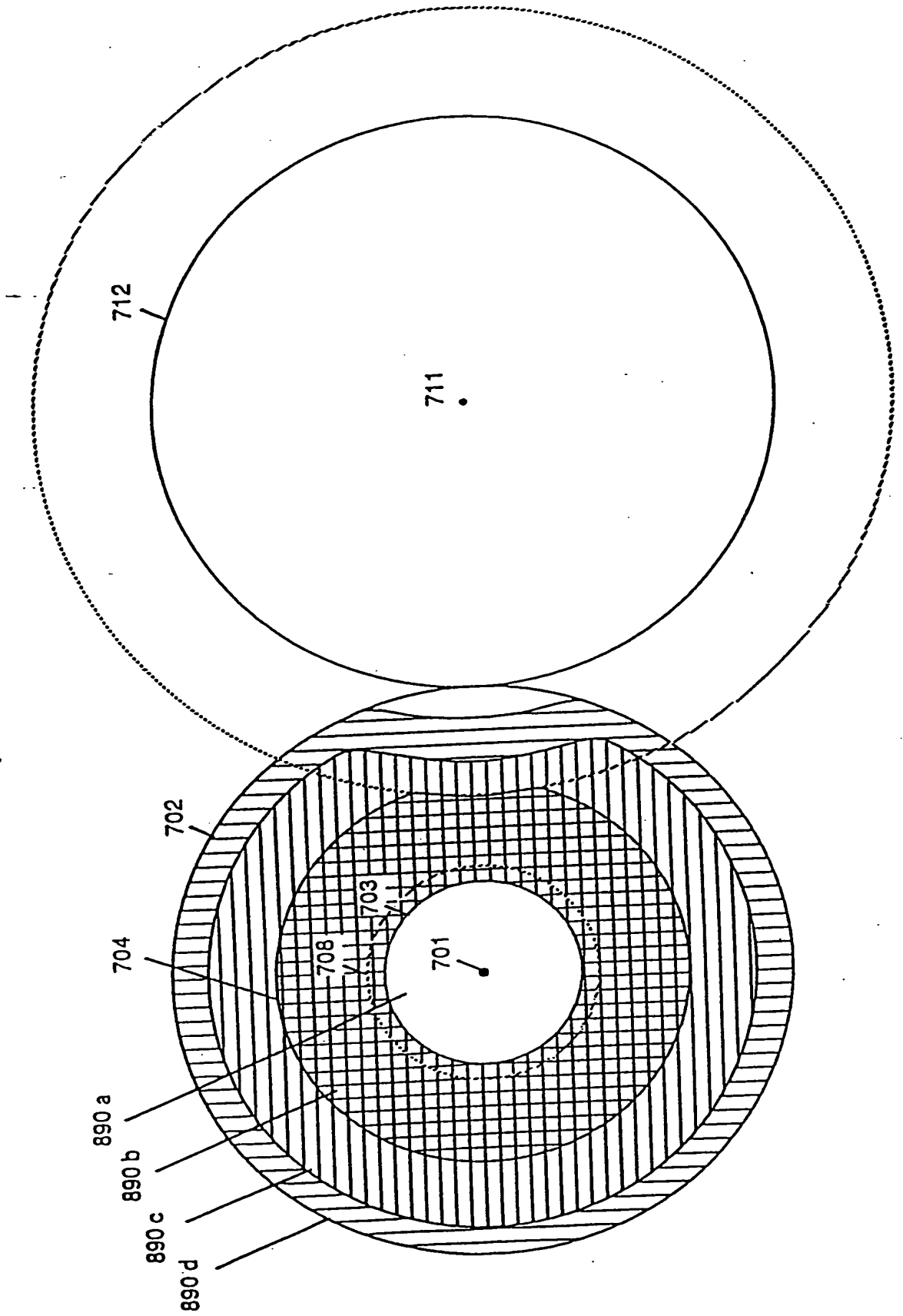


FIG. 92

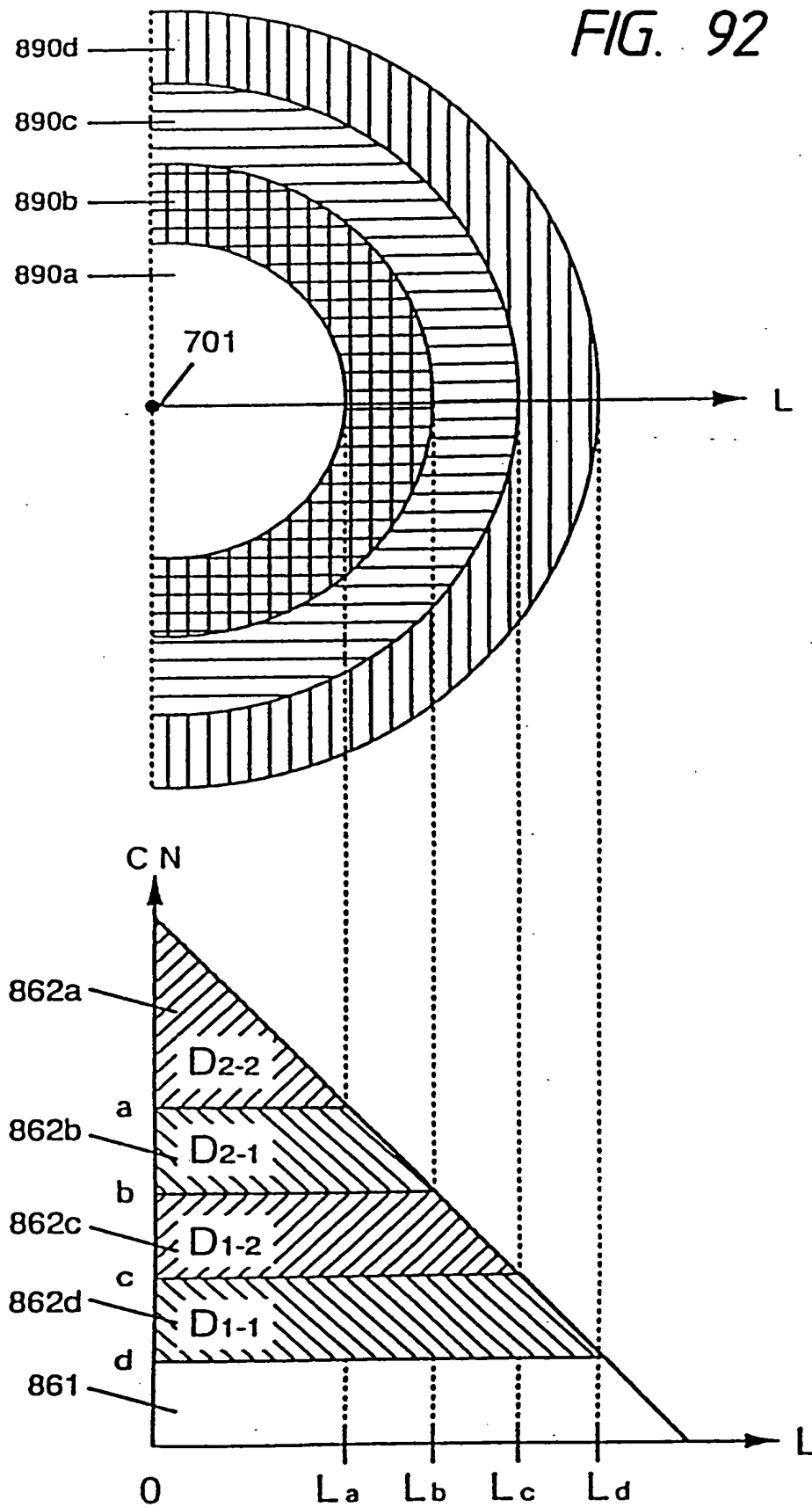


FIG. 93

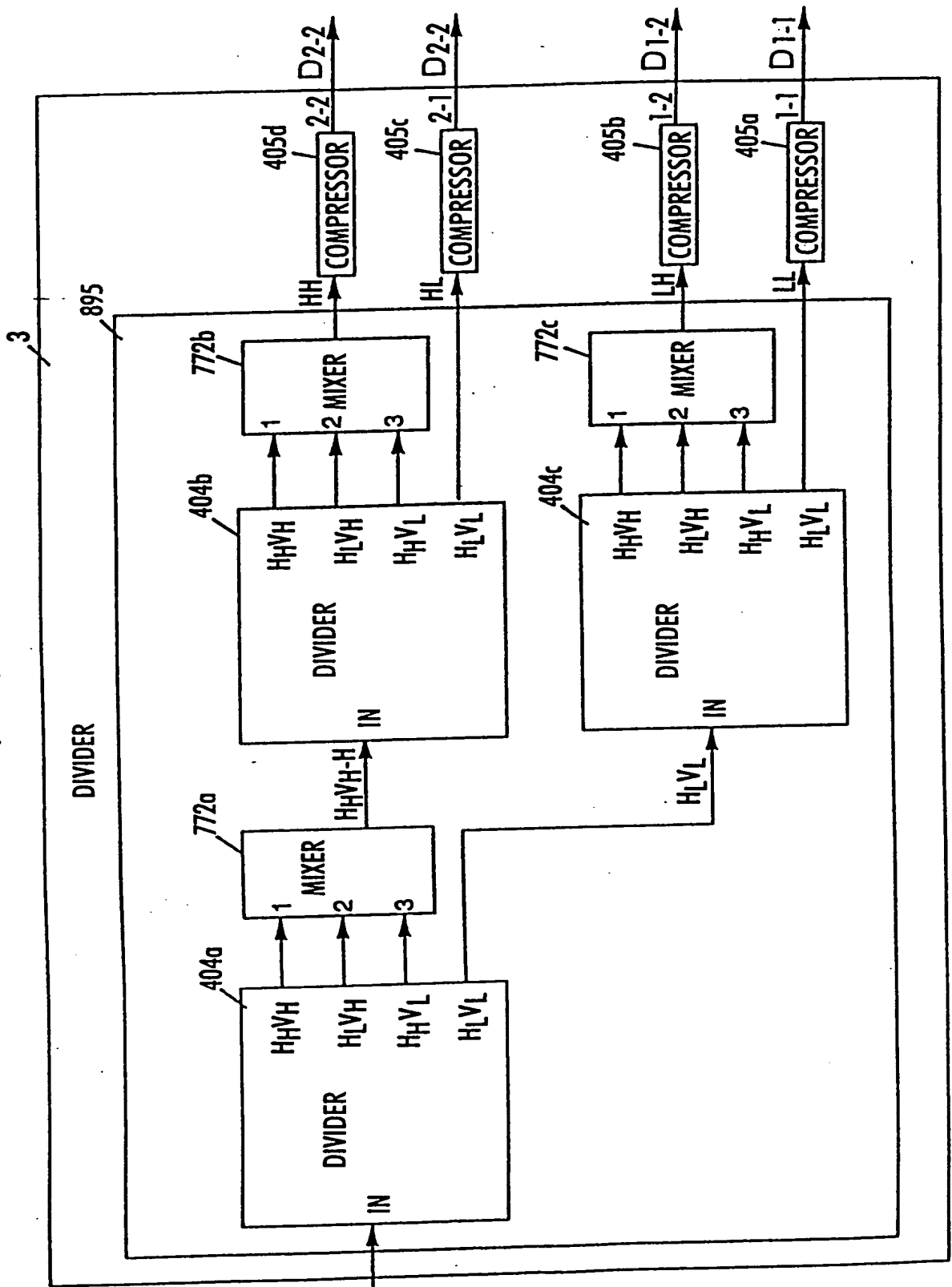


FIG. 94

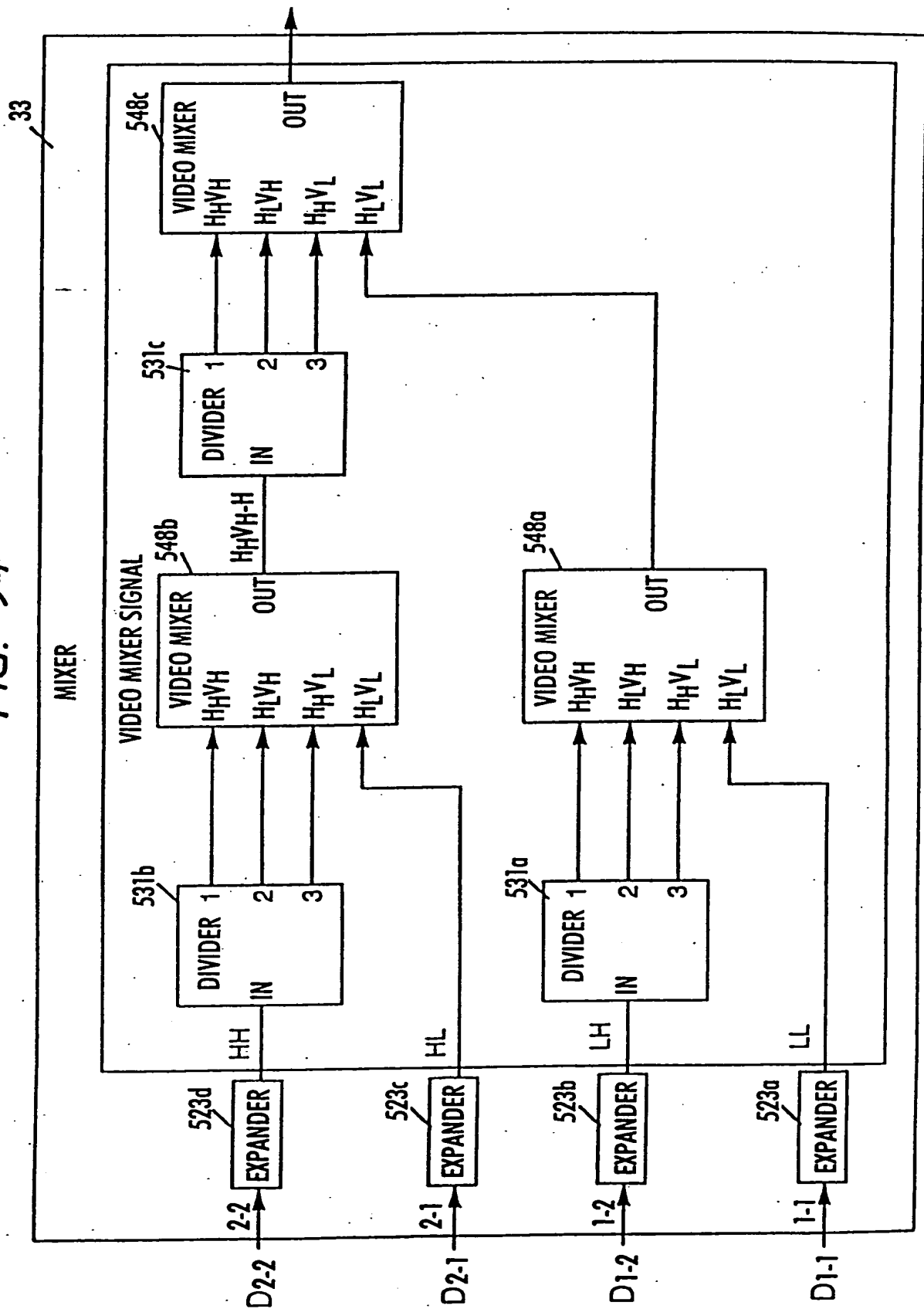


FIG. 95

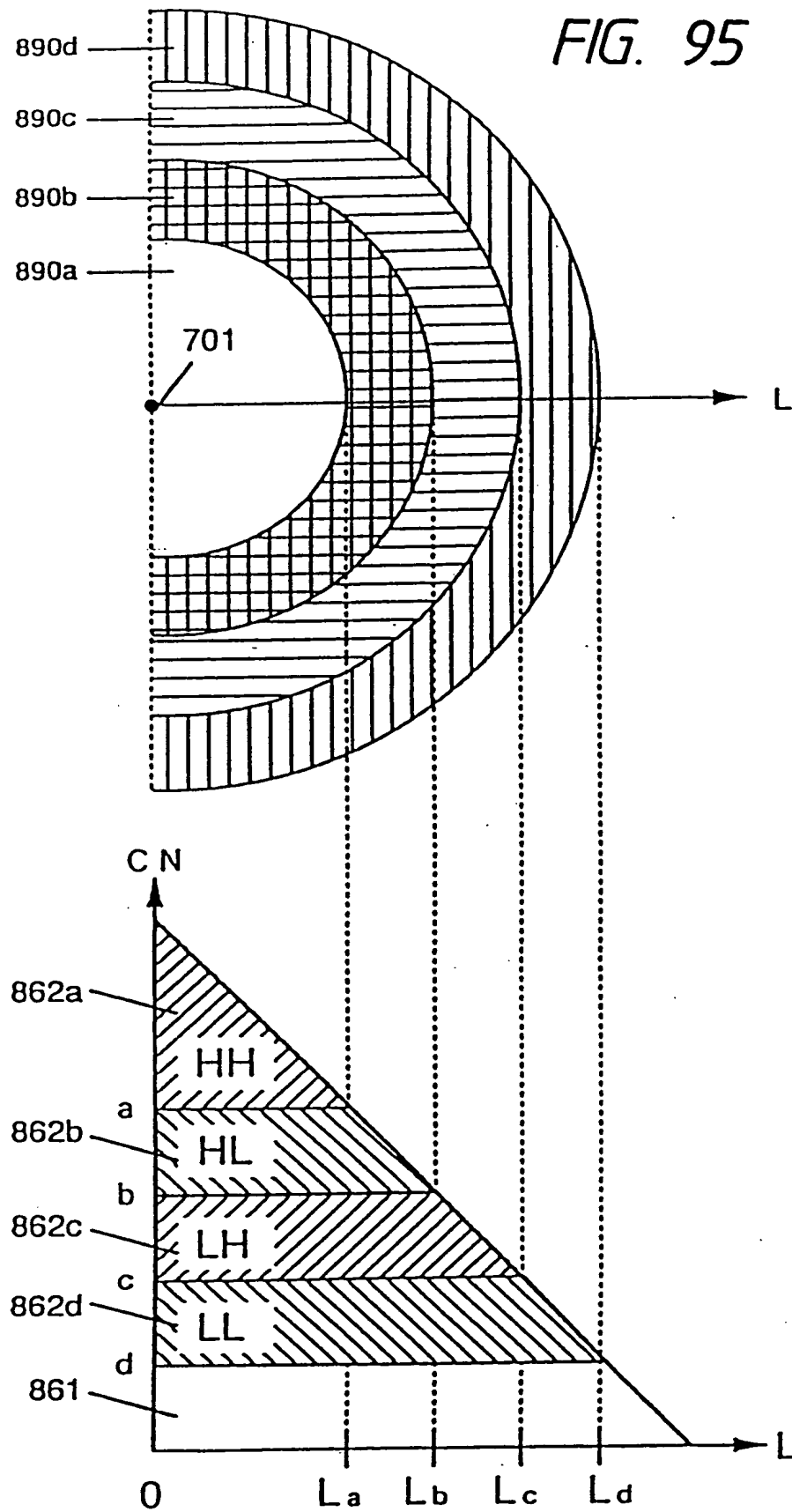


FIG. 96

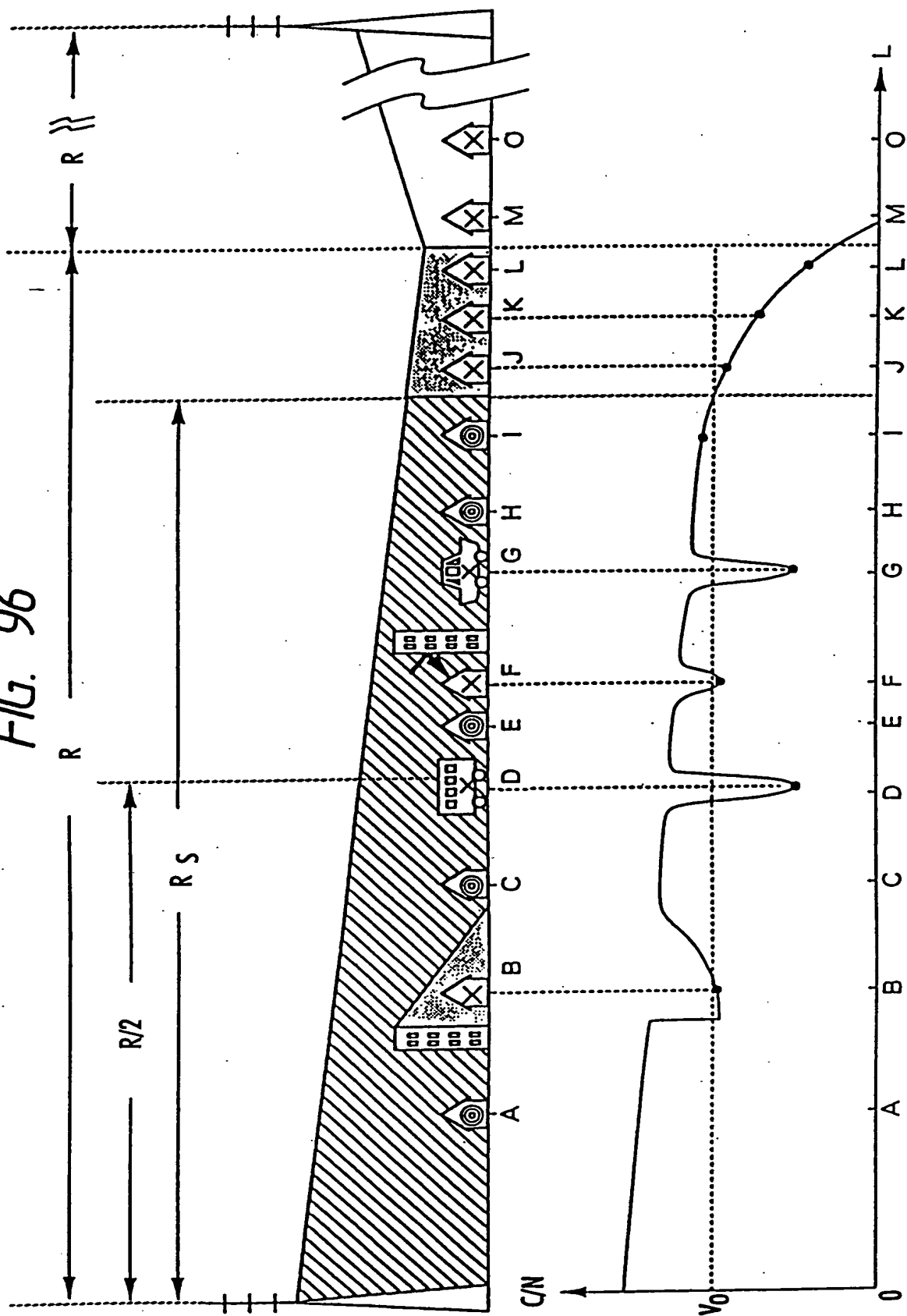




FIG. 97

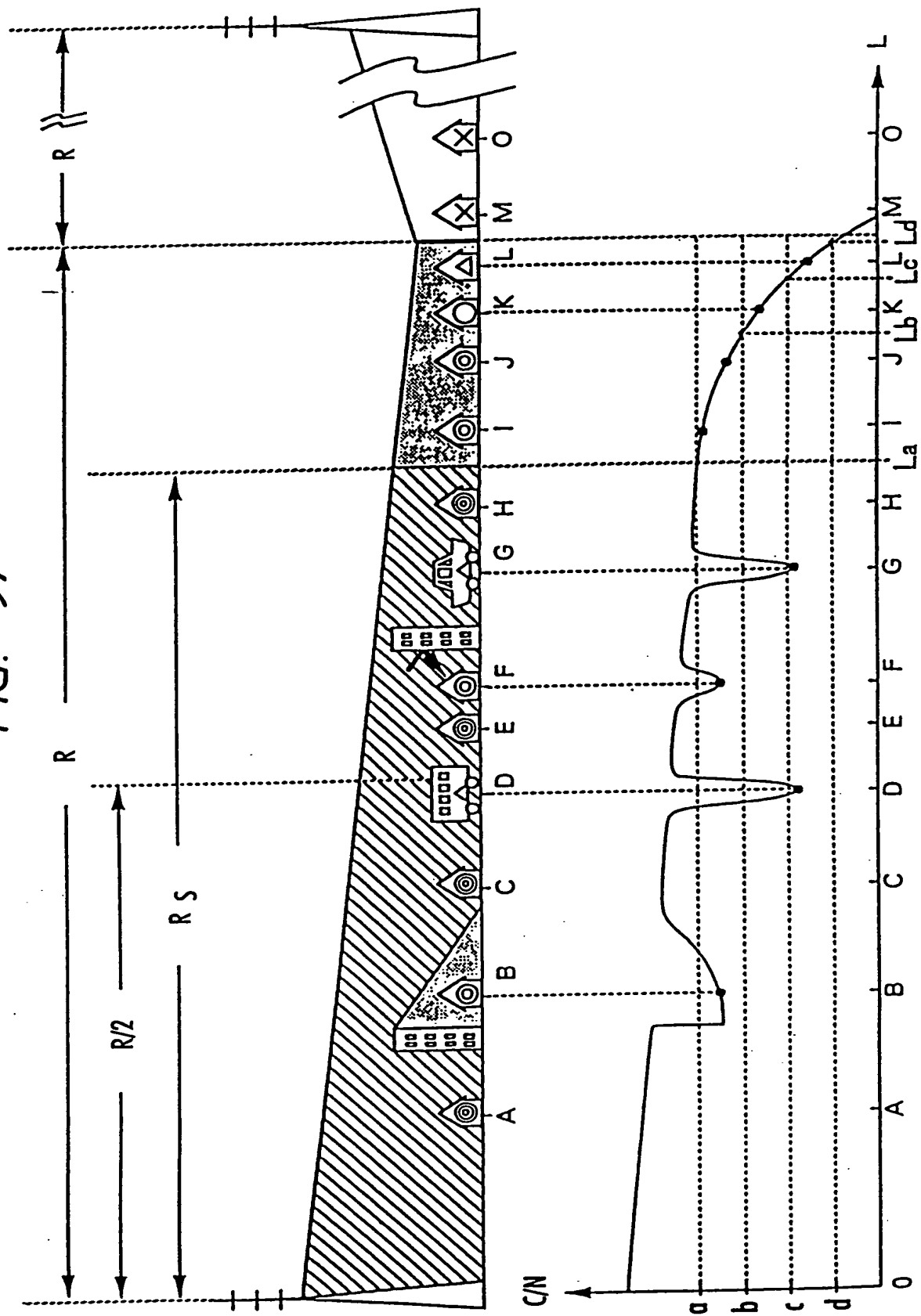


FIG. 98

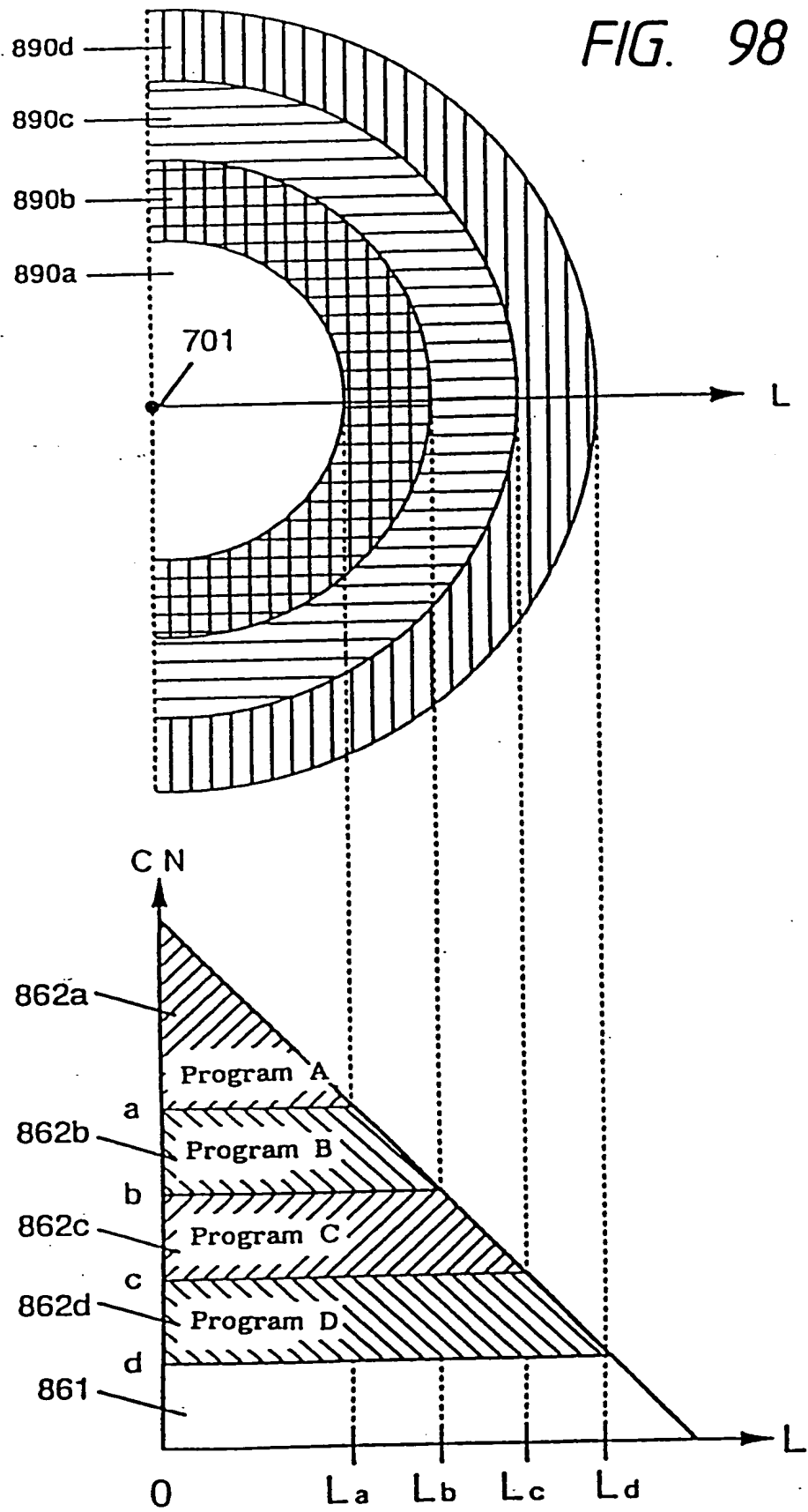


FIG. 99

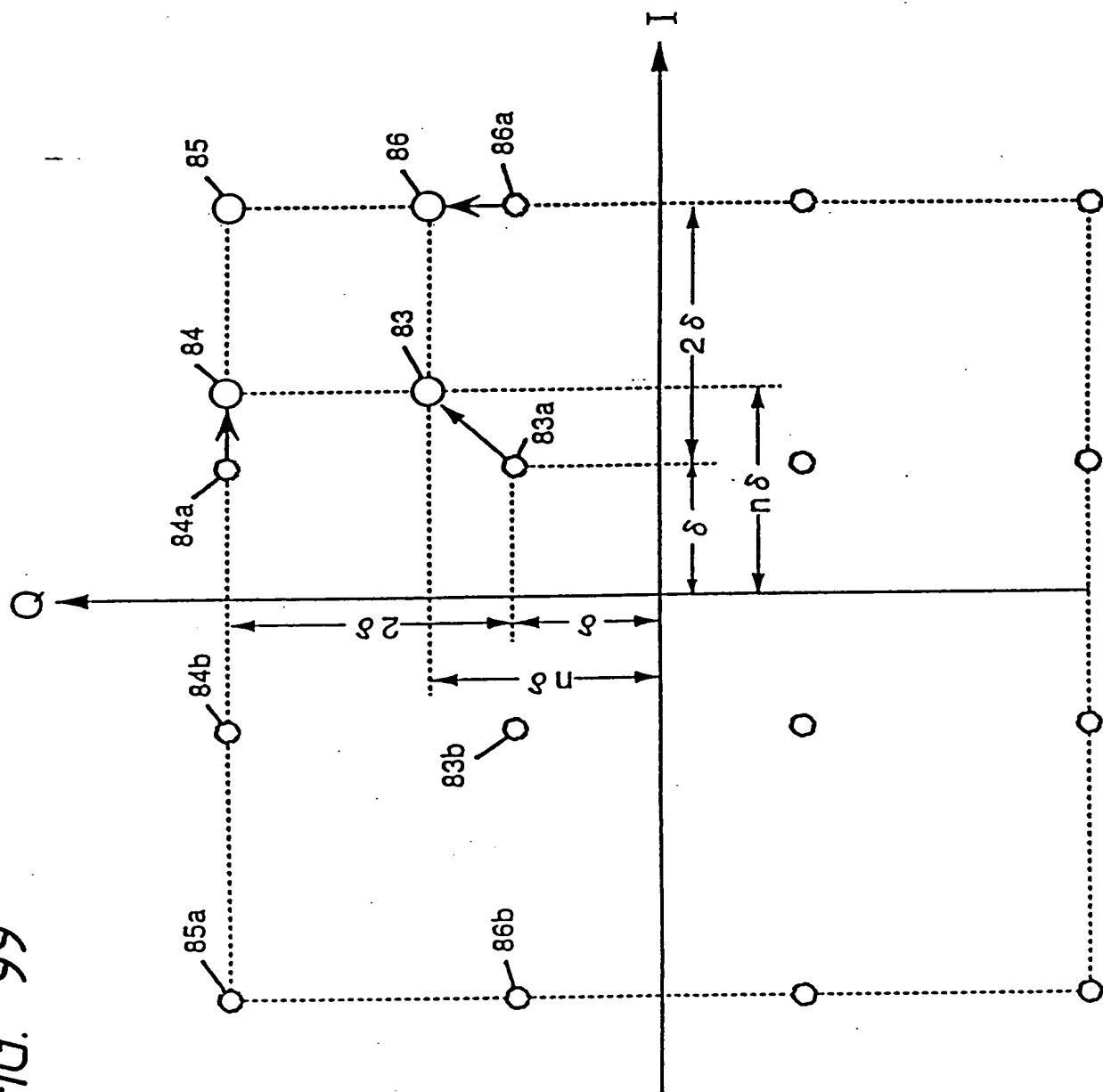


FIG. 100

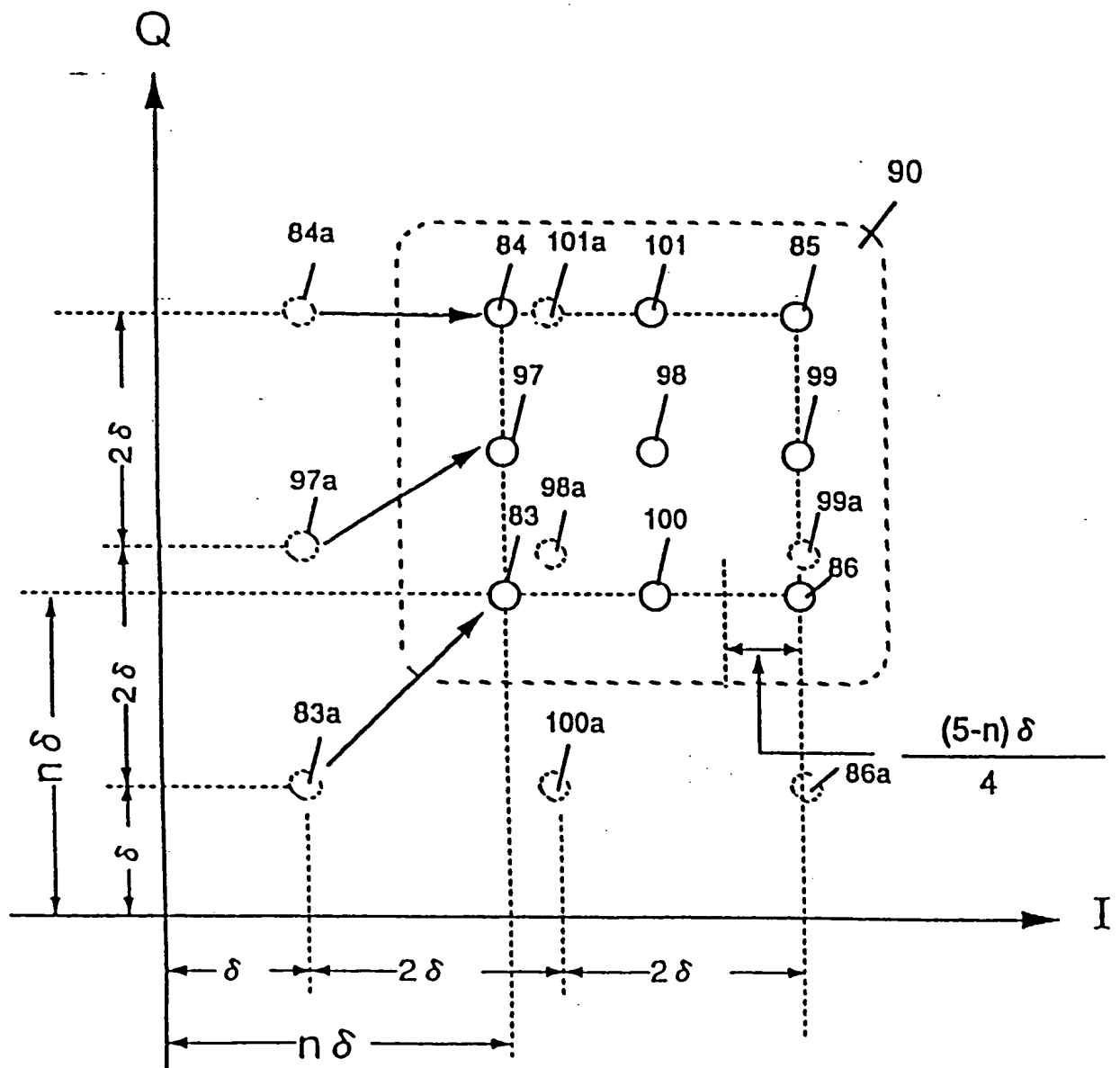


FIG. 101

Pe

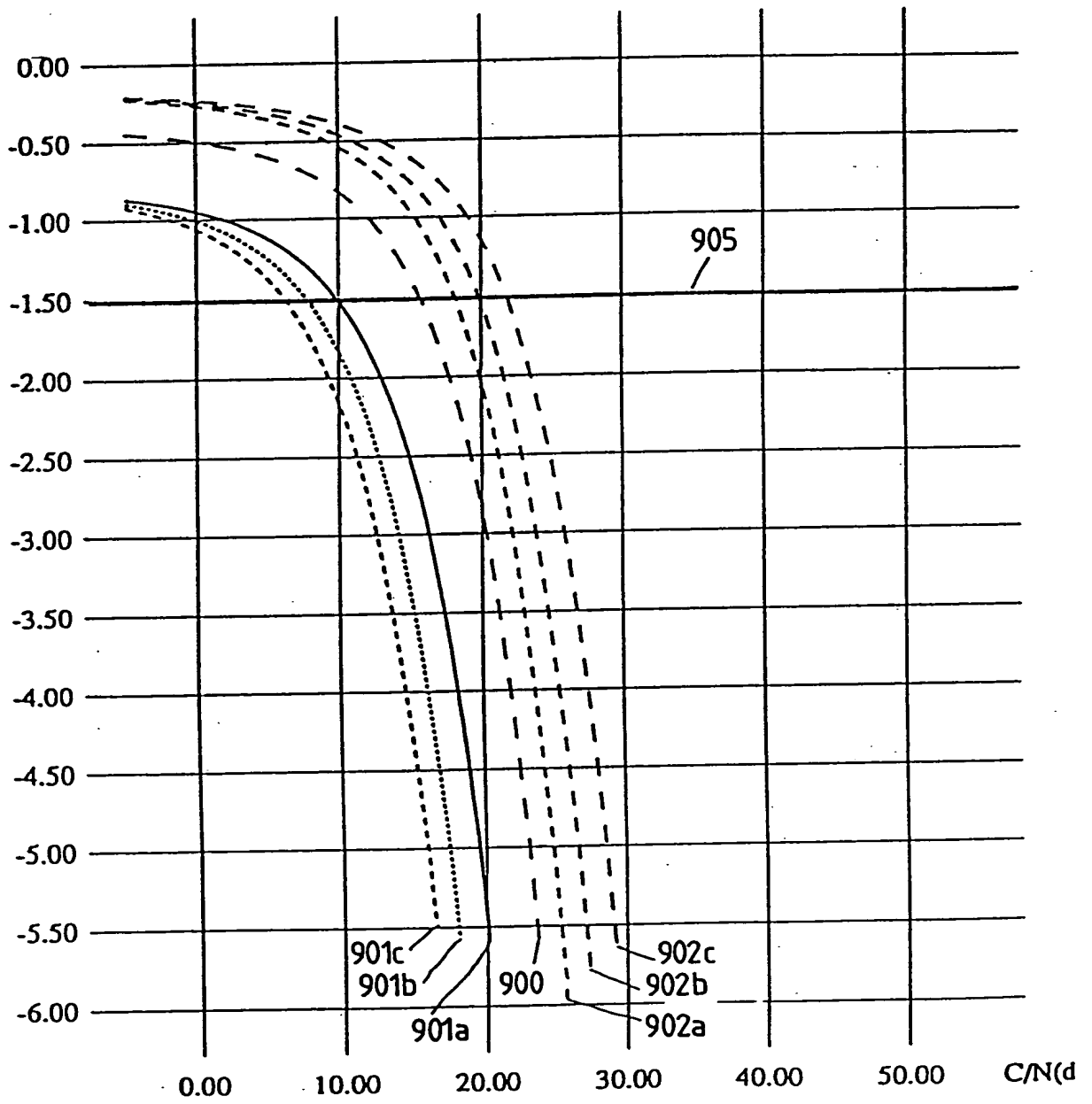


FIG. 102

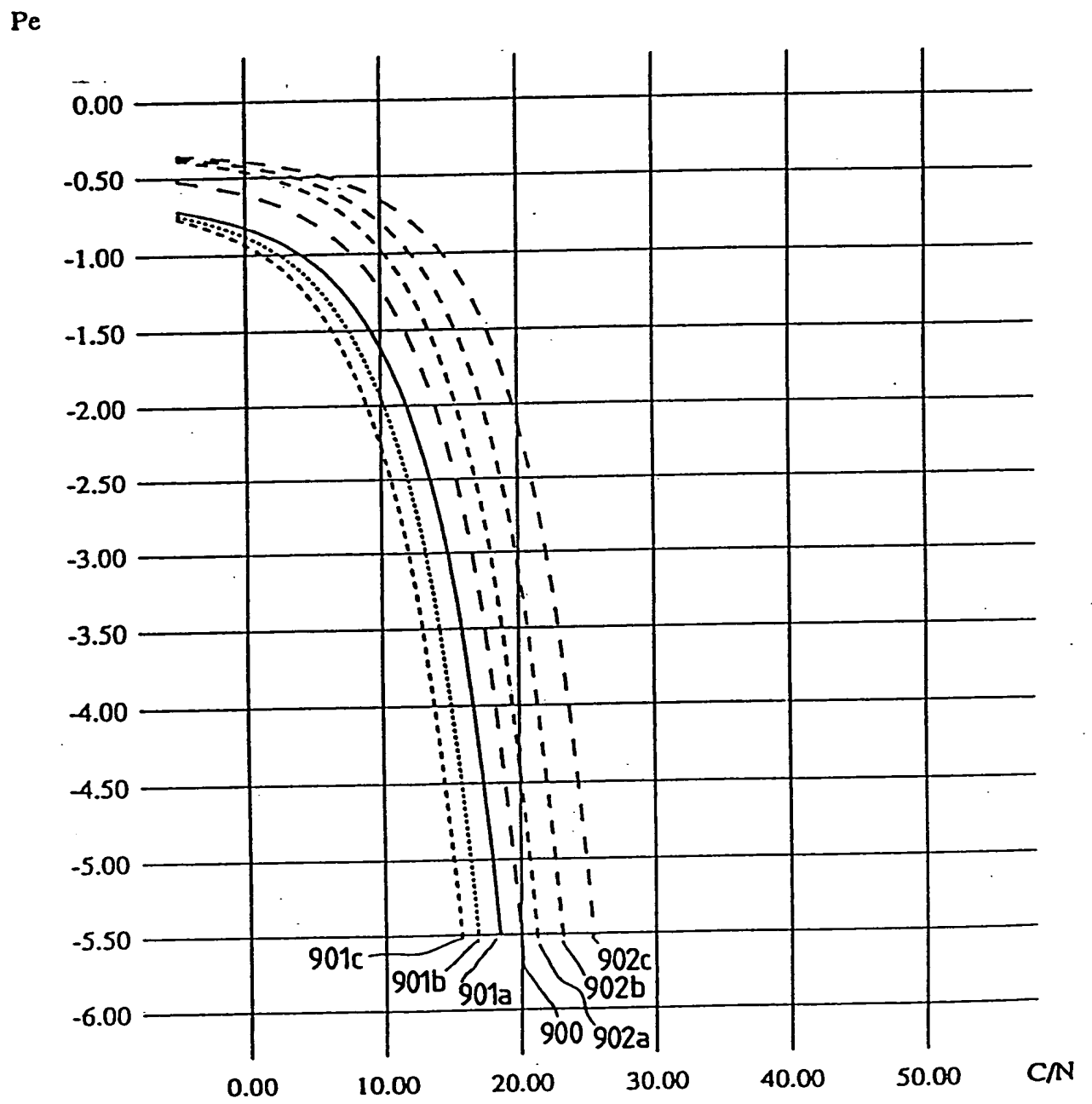


FIG. 103

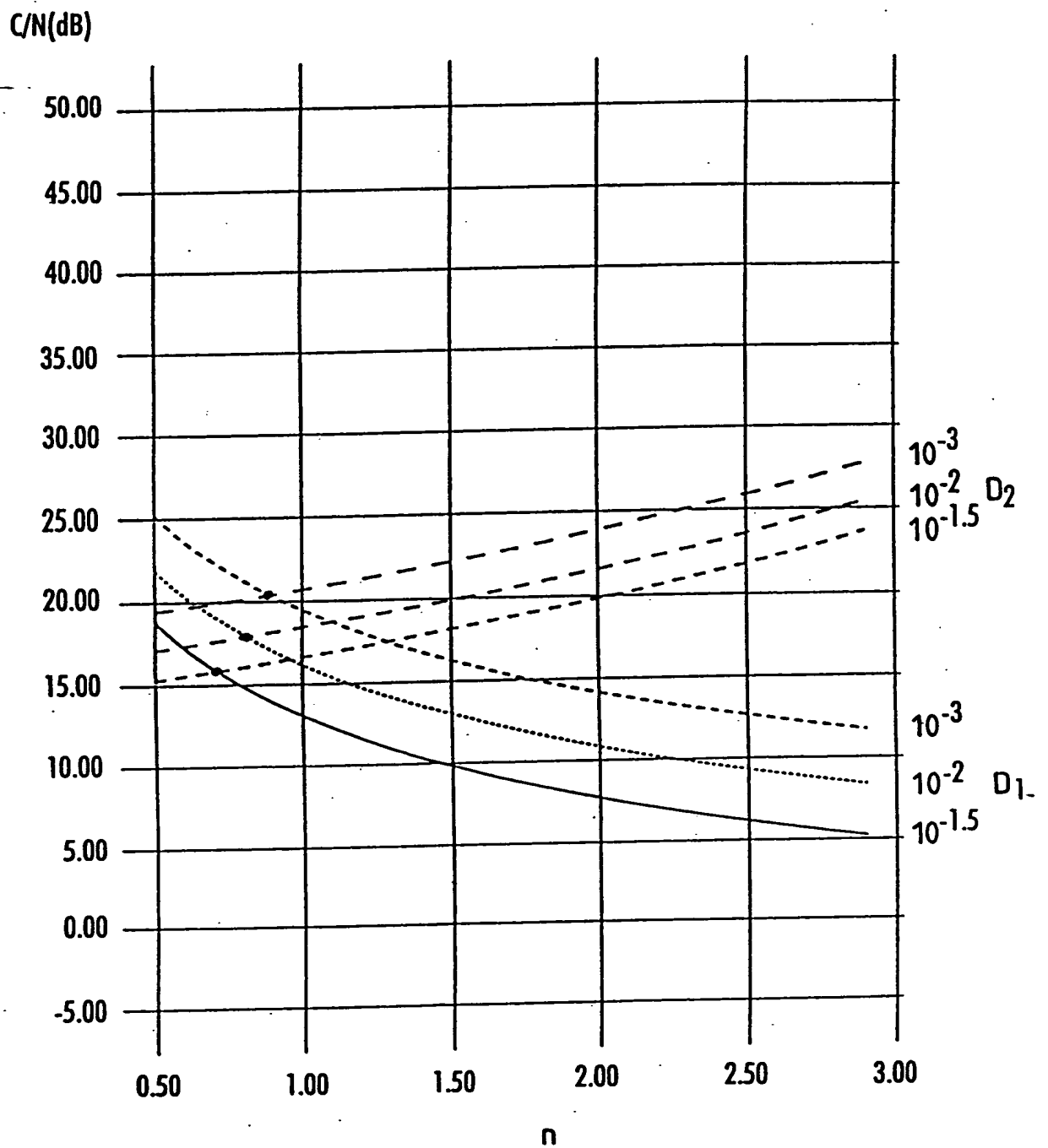


FIG. 104

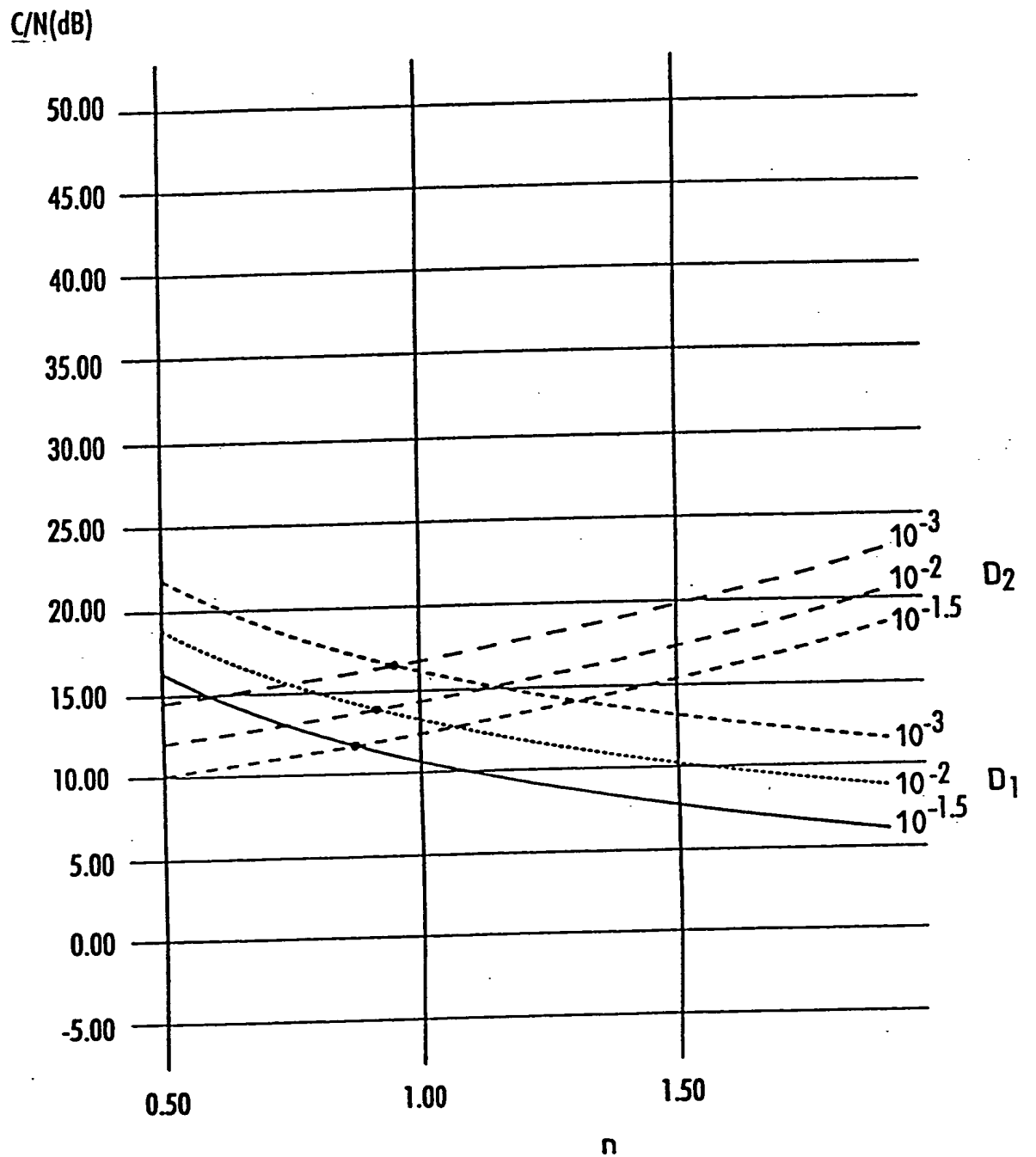
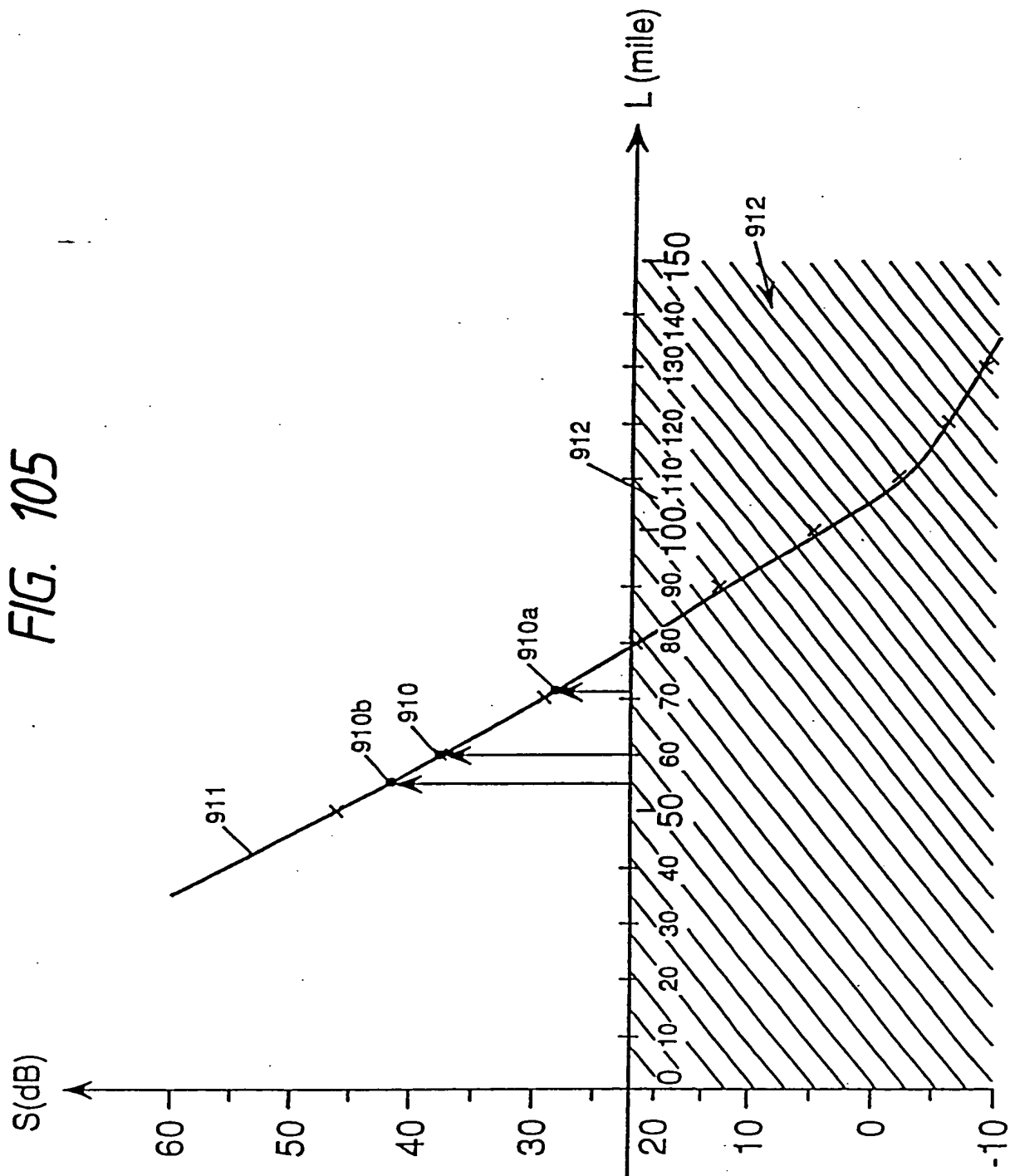
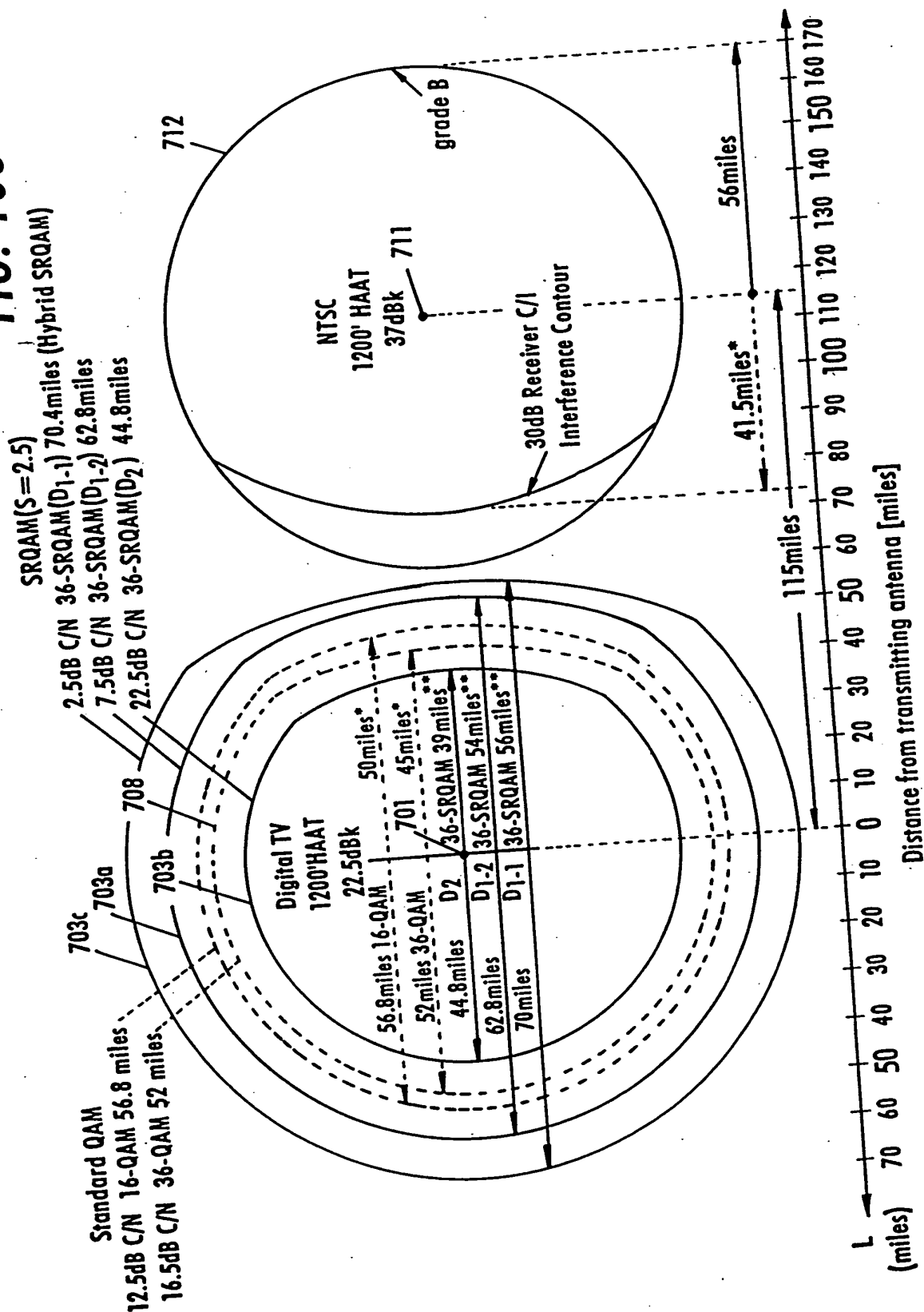




FIG. 105



# FIG. 106



# FIG. 107

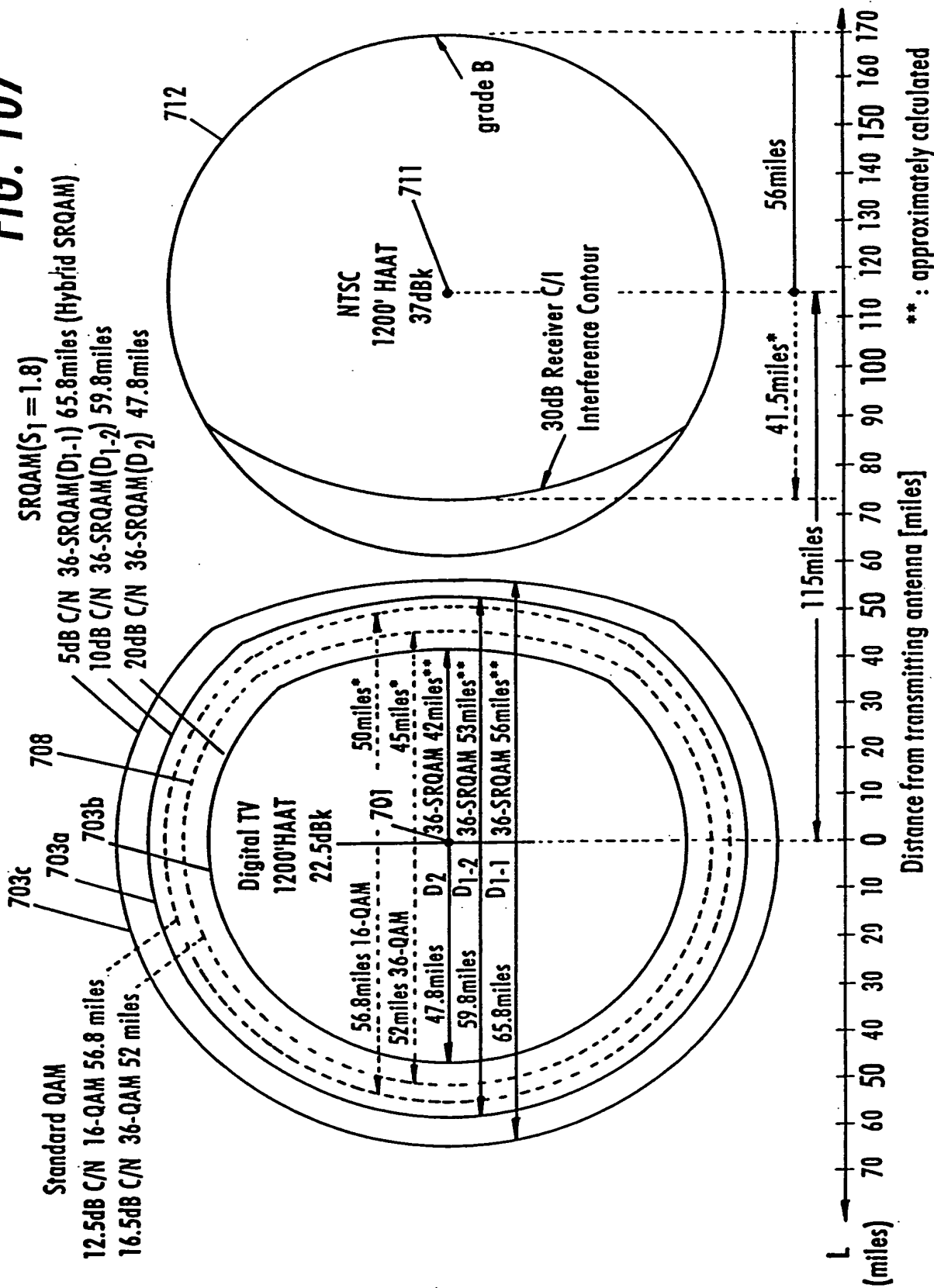


FIG. 108(A)

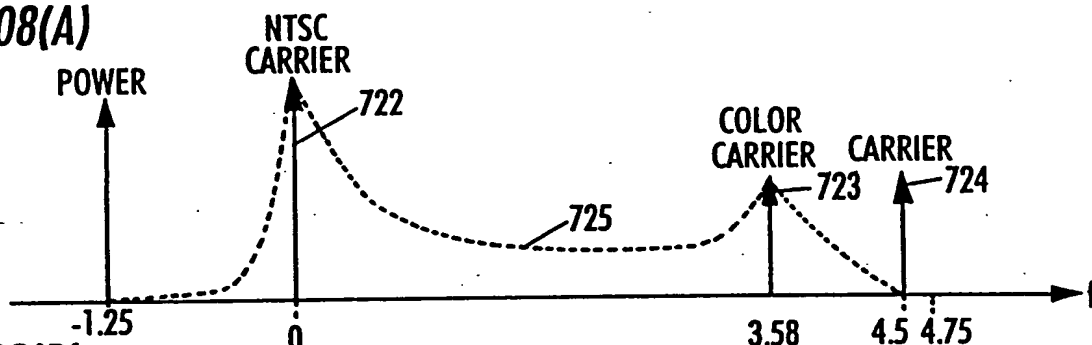


FIG. 108(B)

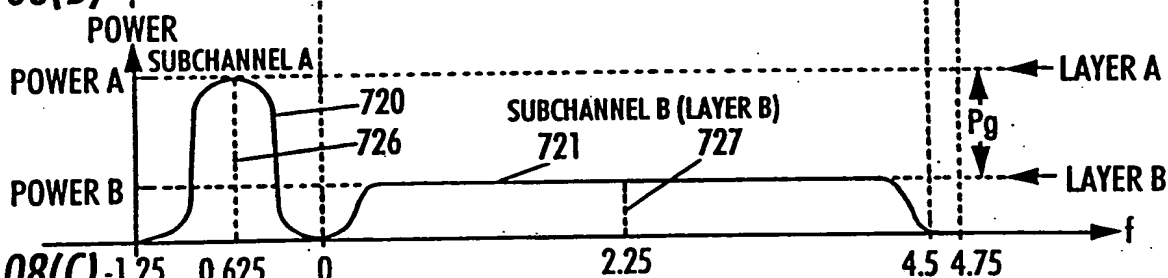


FIG. 108(C)

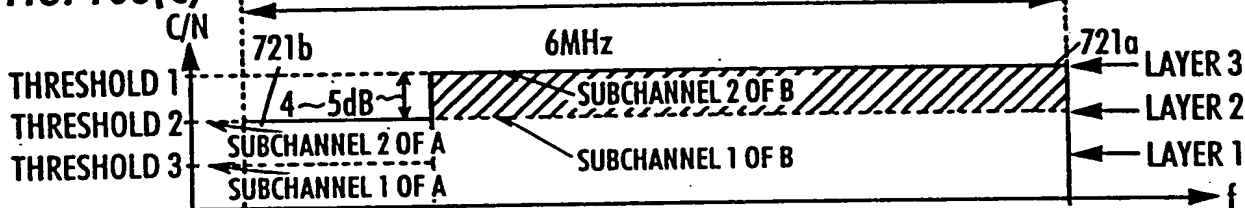


FIG. 108(D)

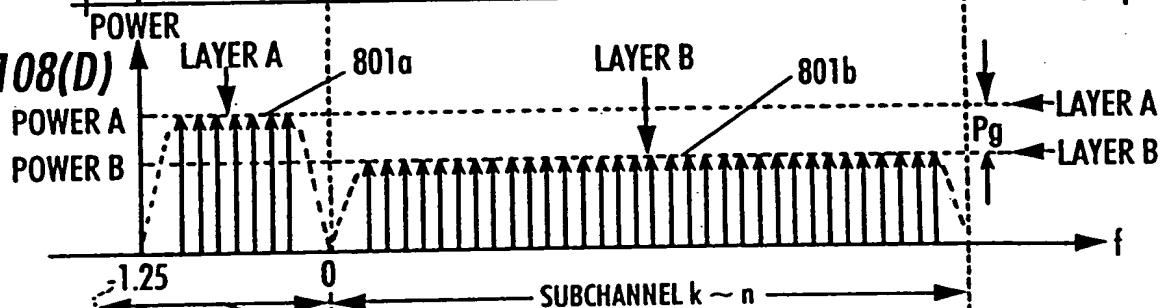


FIG. 108(E)

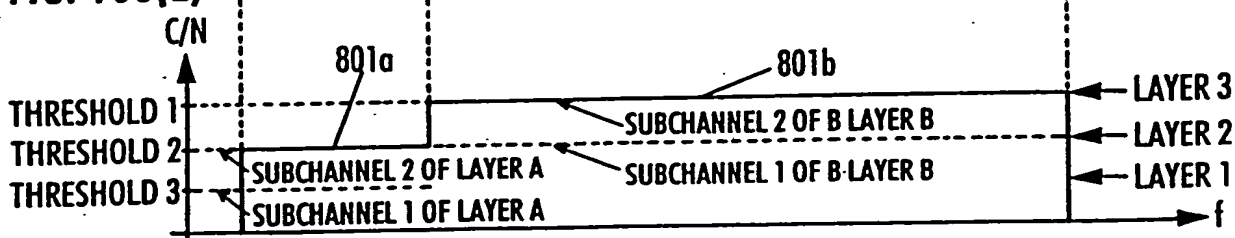


FIG. 109

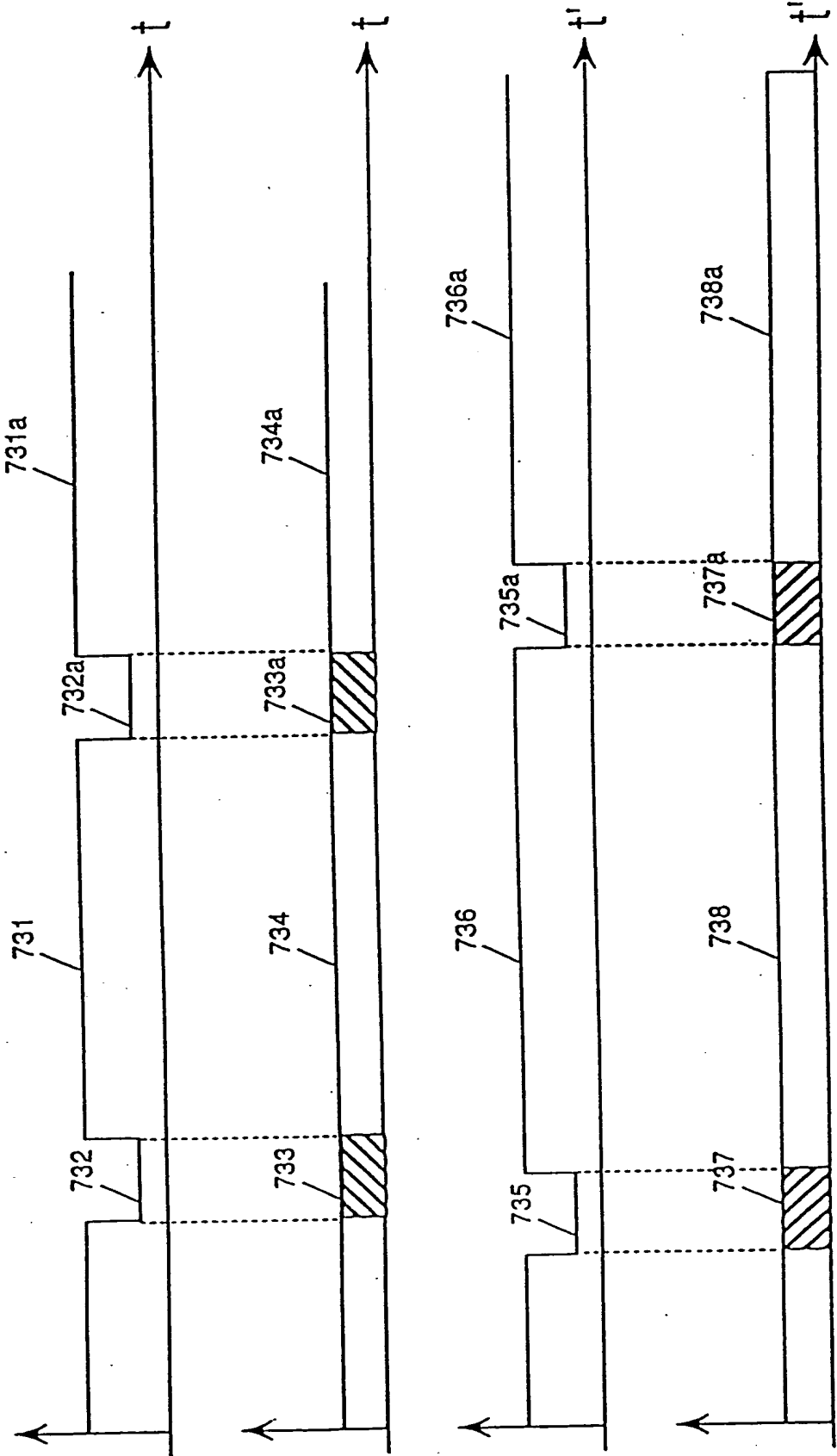
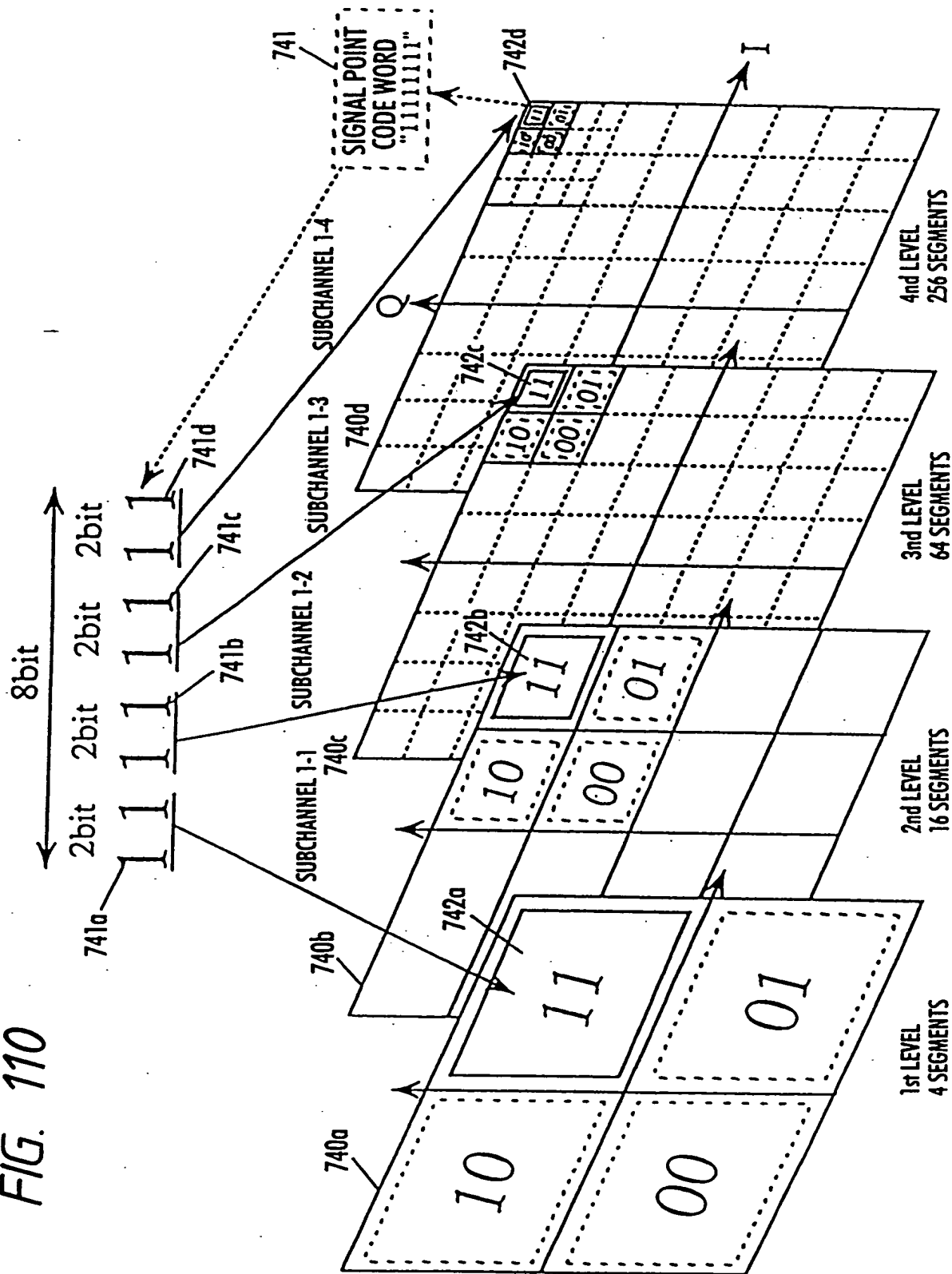
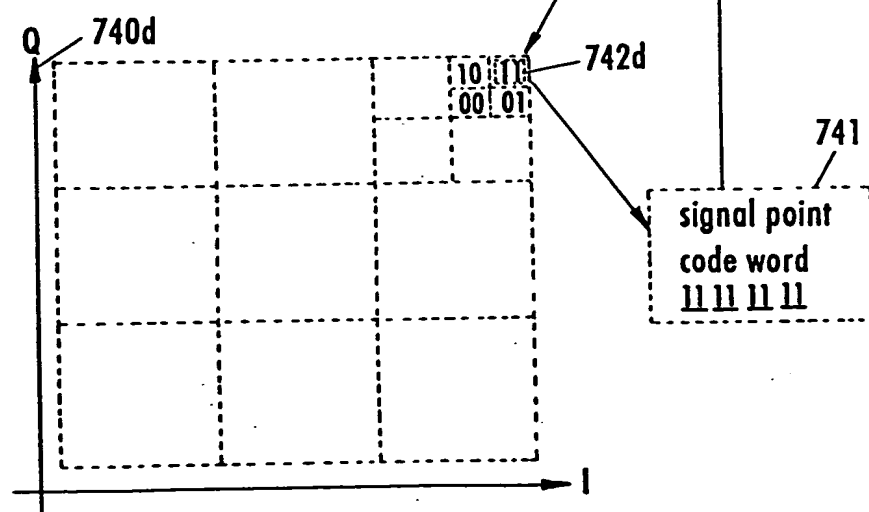
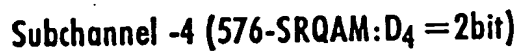


FIG. 110

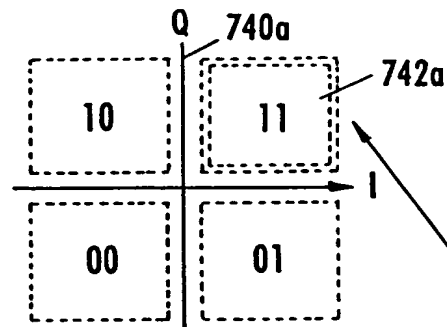


### Subchannel -1 (SRQAM: $D_1 = 2\text{bit}$ )

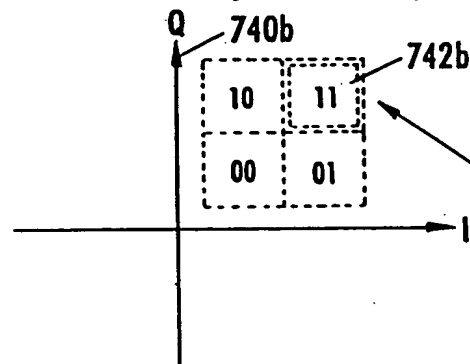


**FIG. 112**

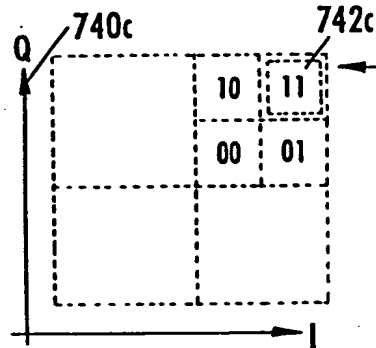
Subchannel -1 (SRQAM:  $D_1 = 2\text{bit}$ )



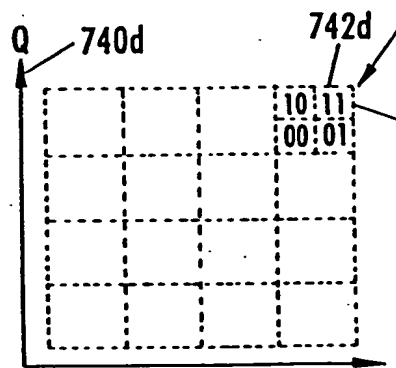
Subchannel -2 (16-SRQAM:  $D_2 = 2\text{bit}$ )



Subchannel -3 (64-SRQAM:  $D_3 = 2\text{bit}$ )



Subchannel -4 (256-SRQAM:  $D_4 = 2\text{bit}$ )



code word-1

code word-2

code word-3

code word-4

741a

741b

741c

741d

2bit

2bit

2bit

2bit

8bit

signal point  
code word  
11 11 11 11

741



FIG. 113

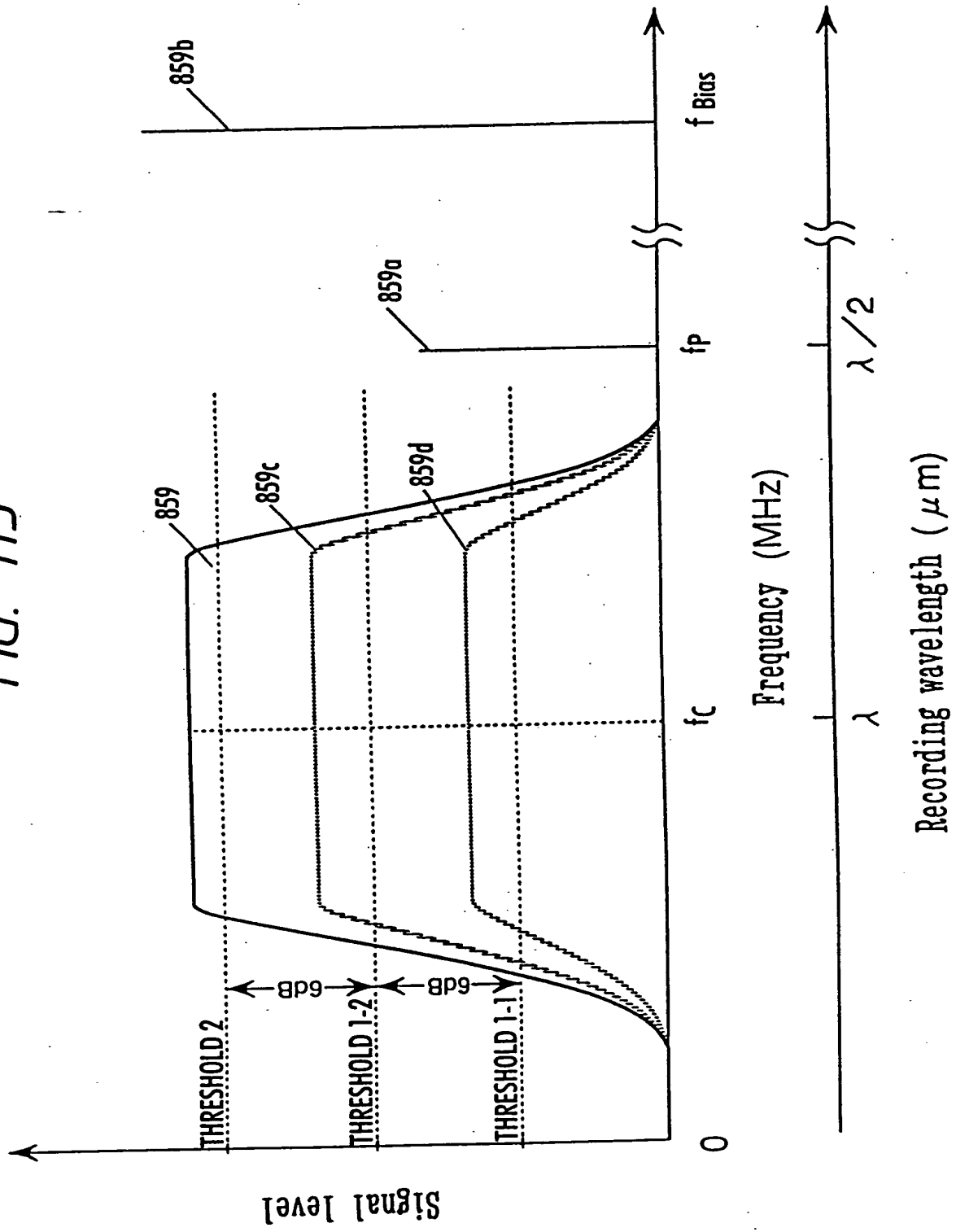


FIG. 114

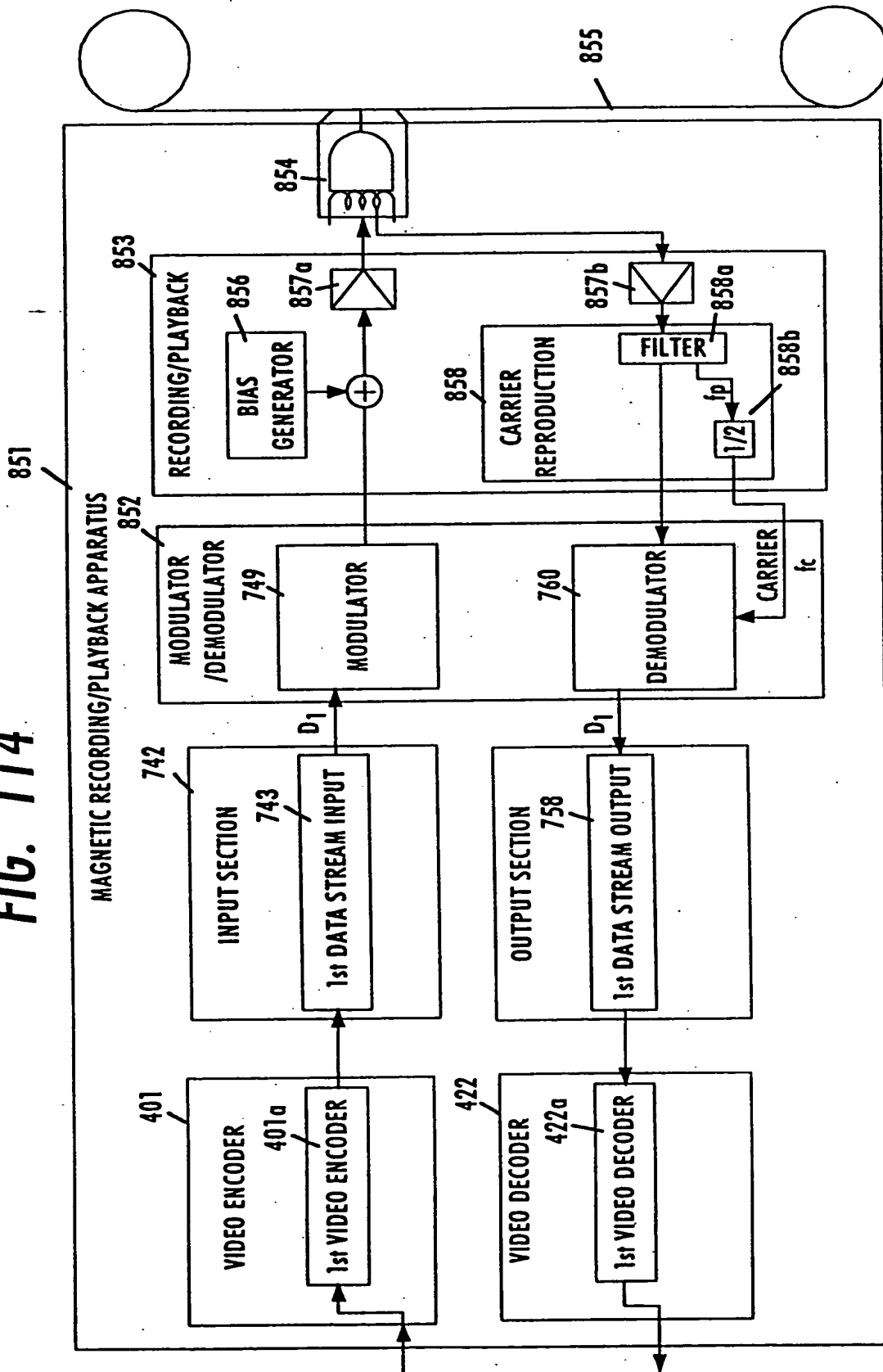


FIG. 115

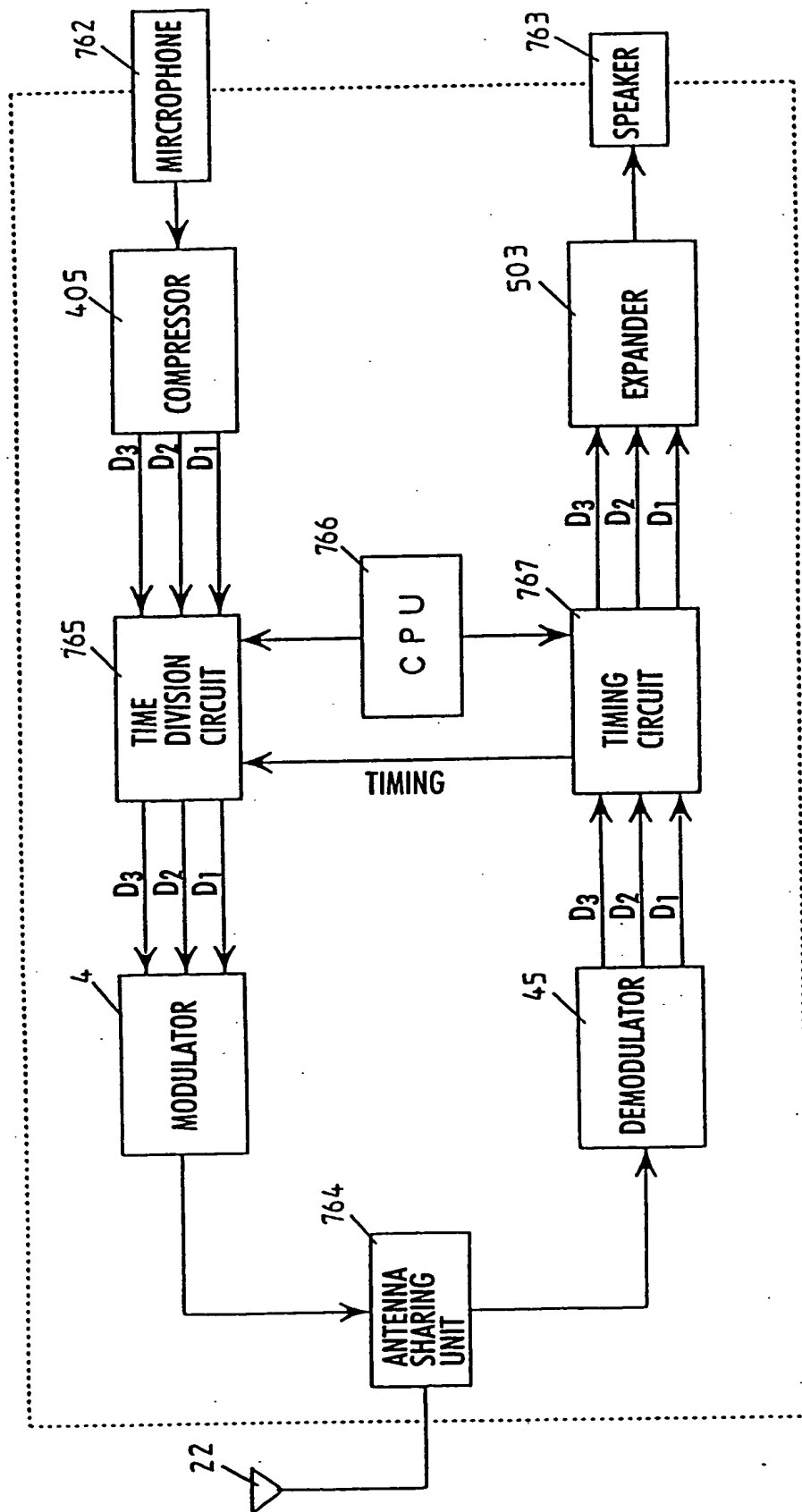


FIG. 116

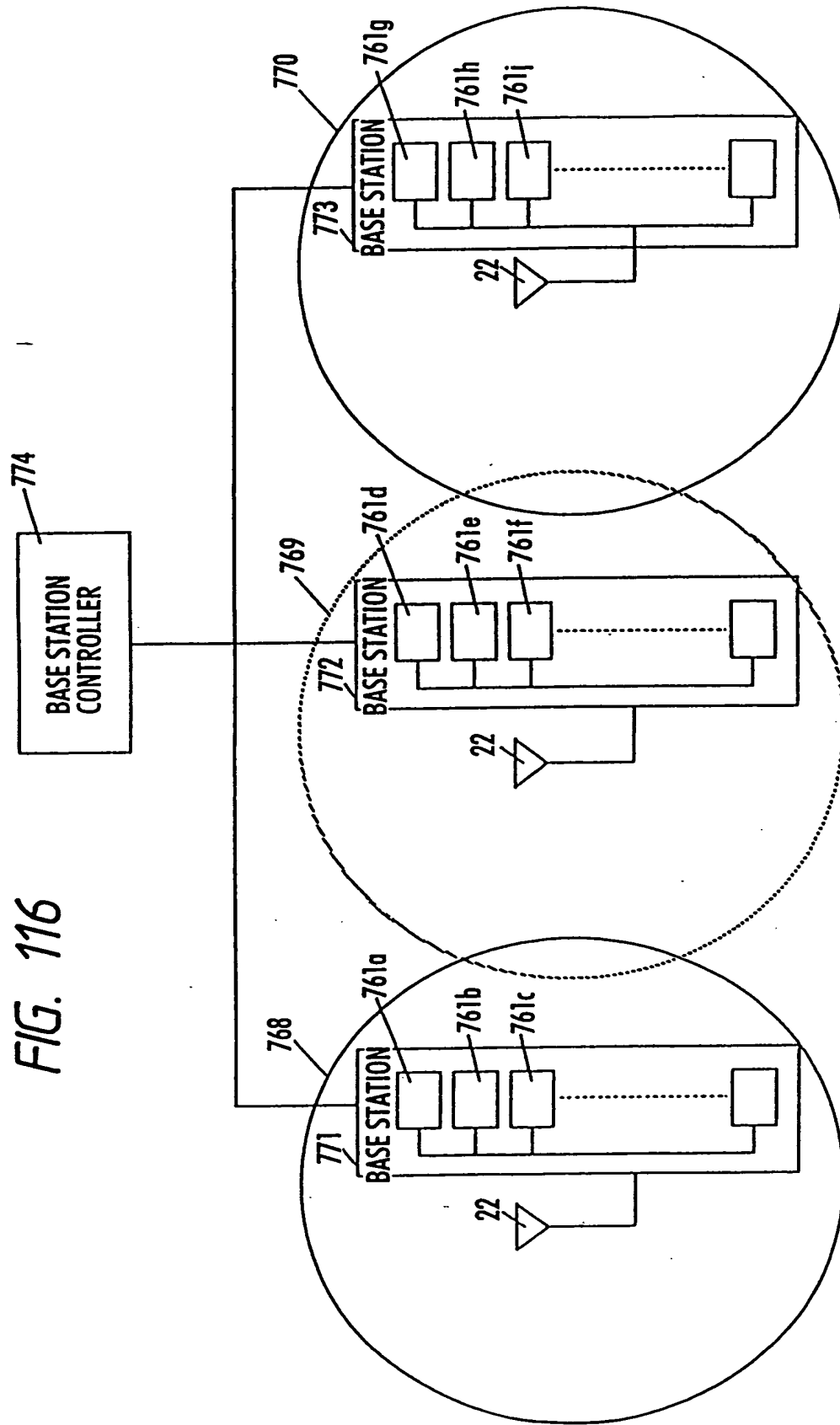


FIG. 117

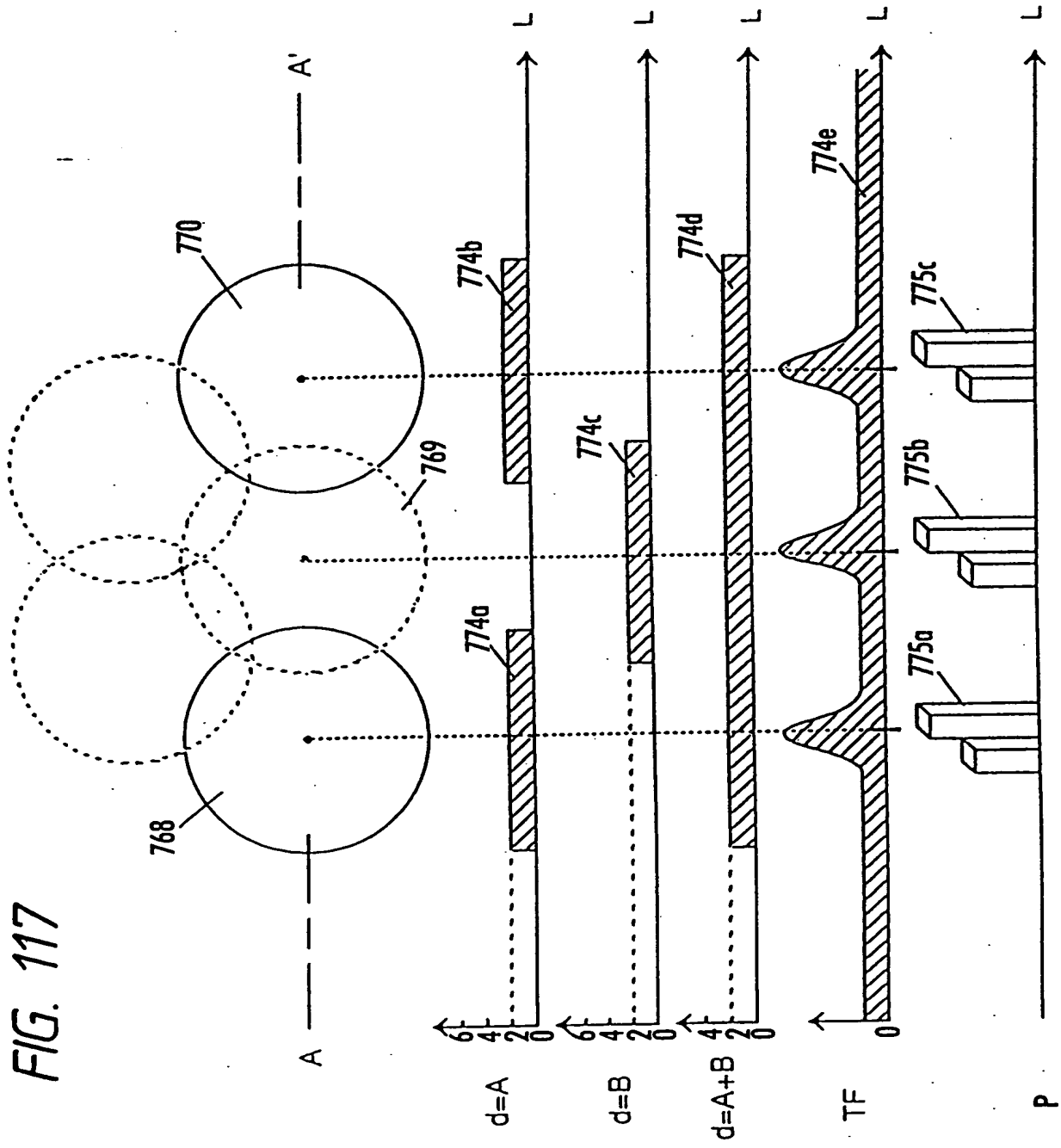


FIG. 118

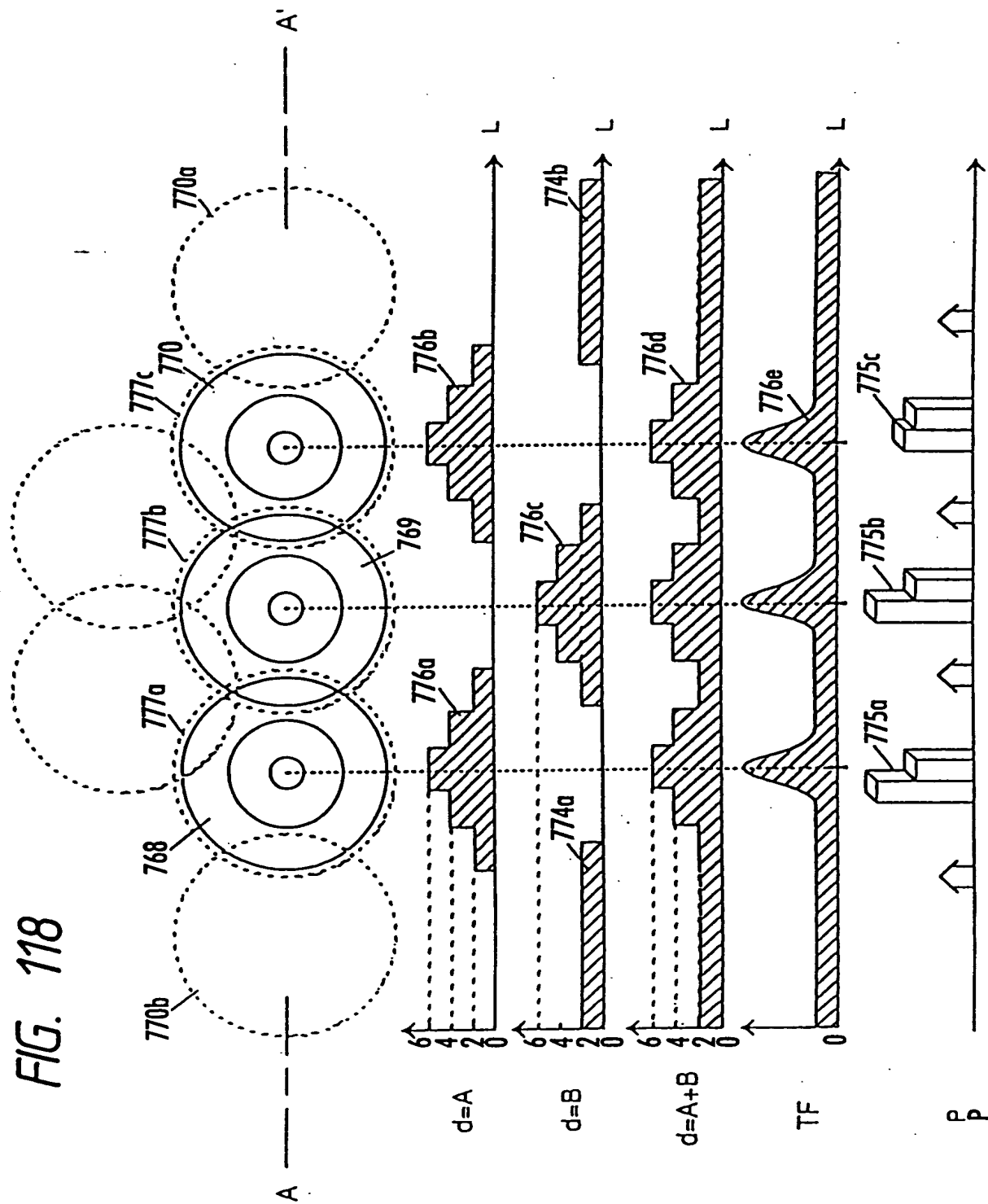


FIG. 119(a)

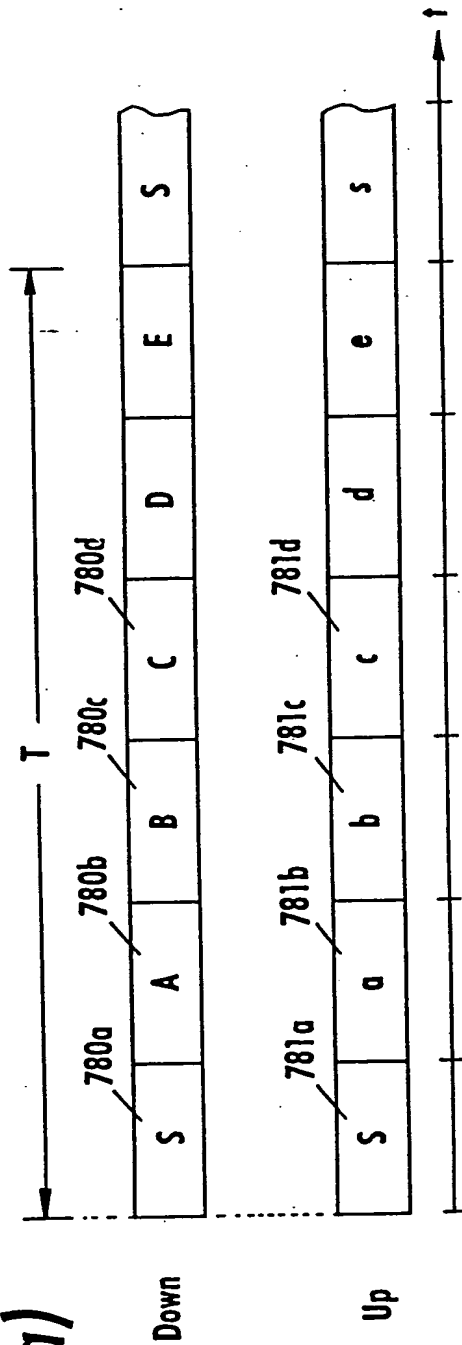


FIG. 119(b)

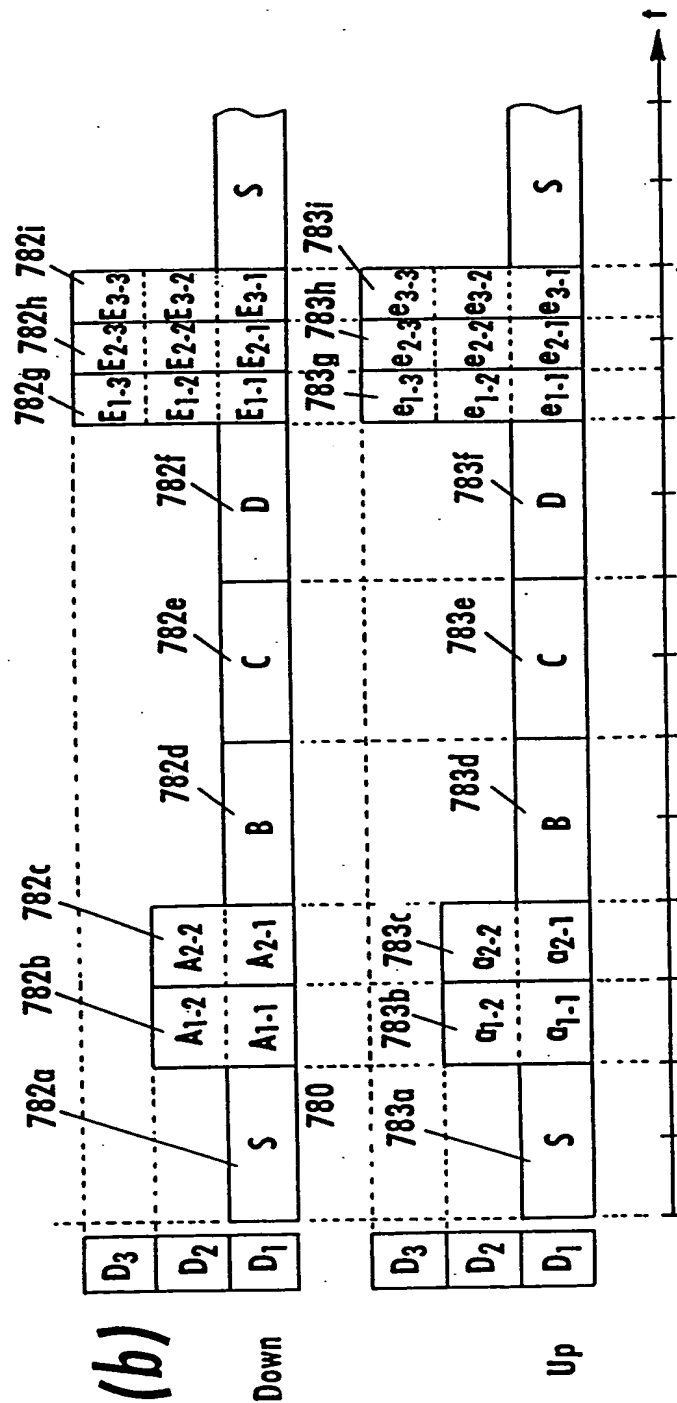






FIG. 121

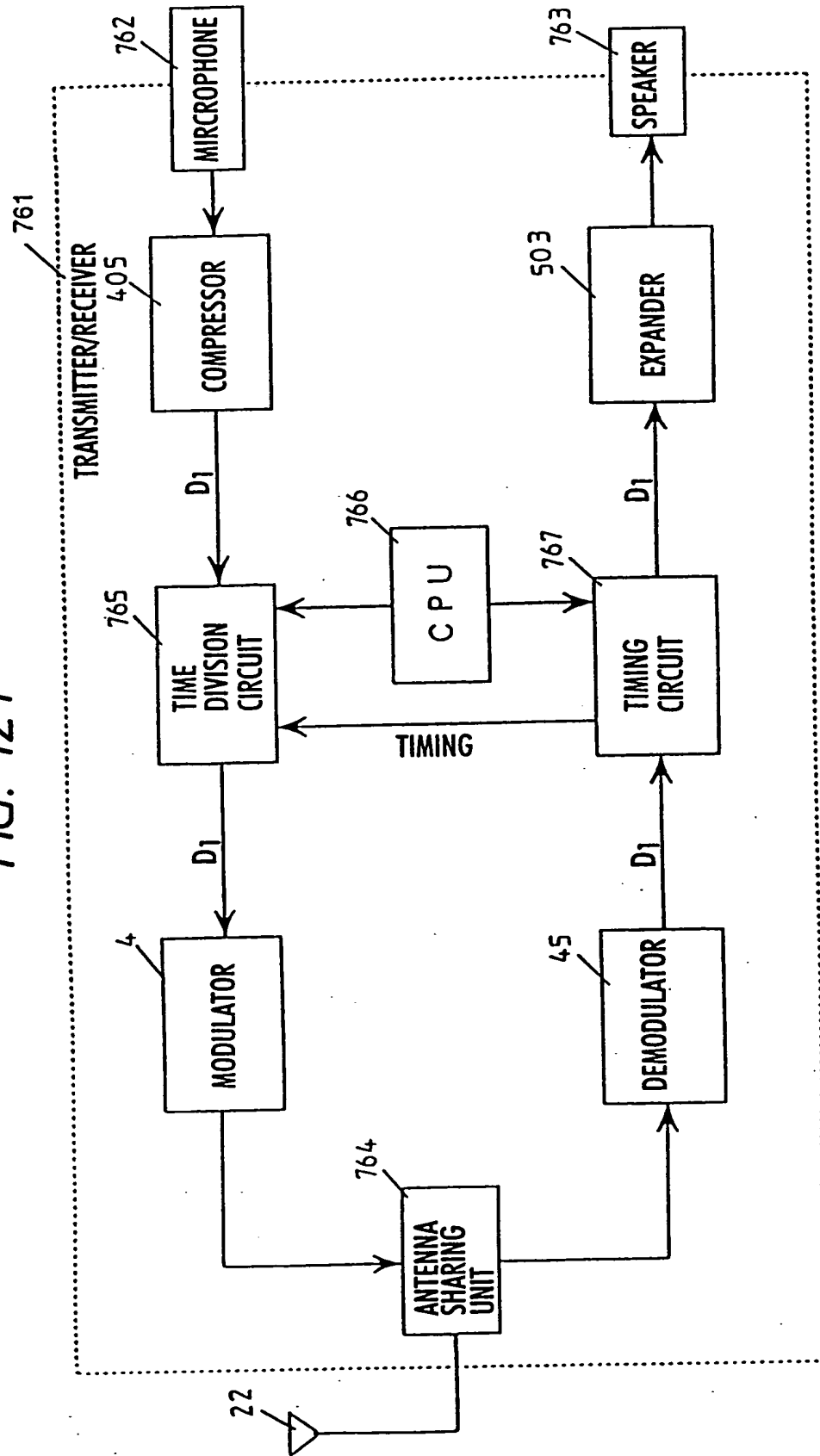
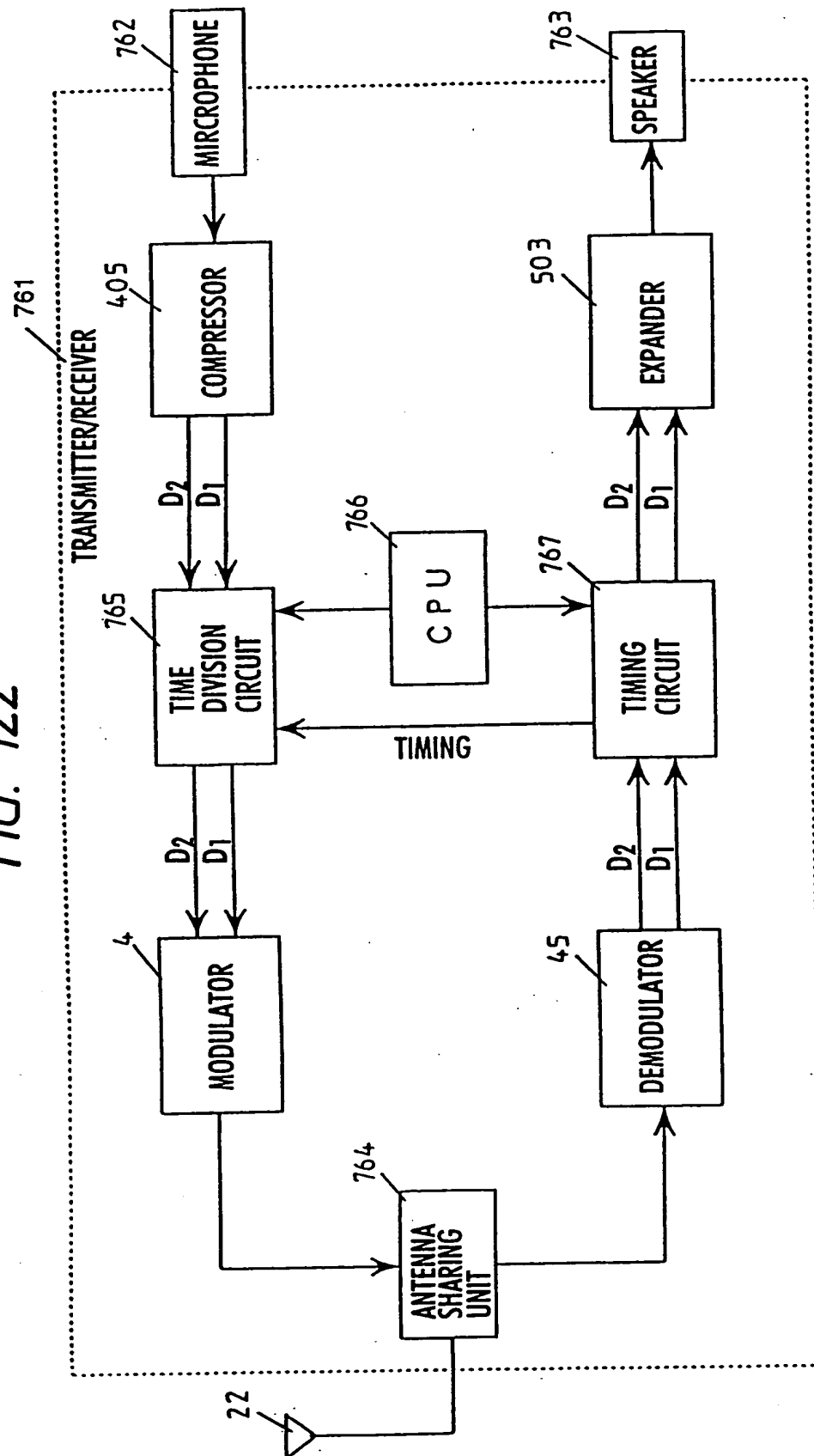


FIG. 122



# FIG. 123

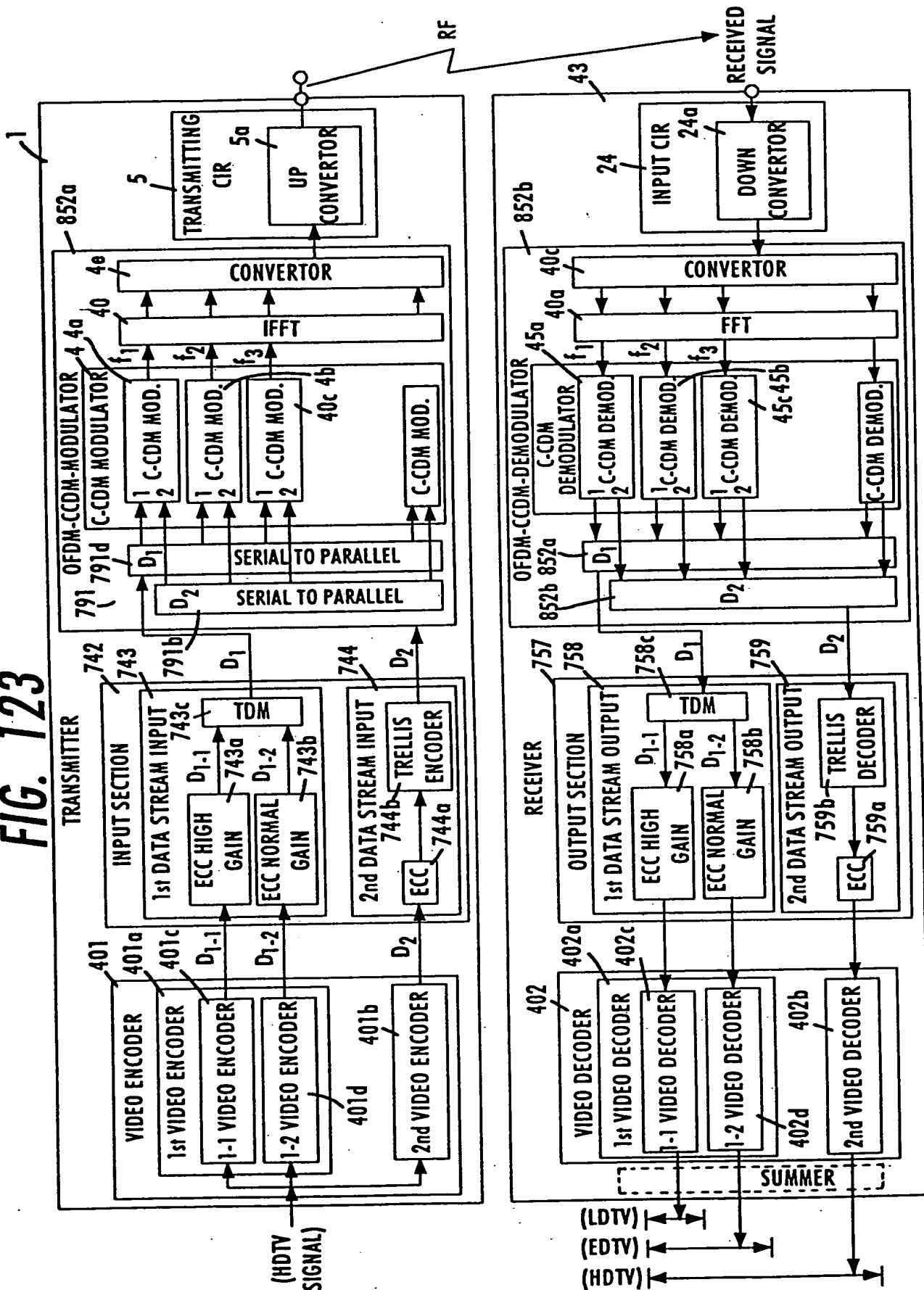


FIG. 124

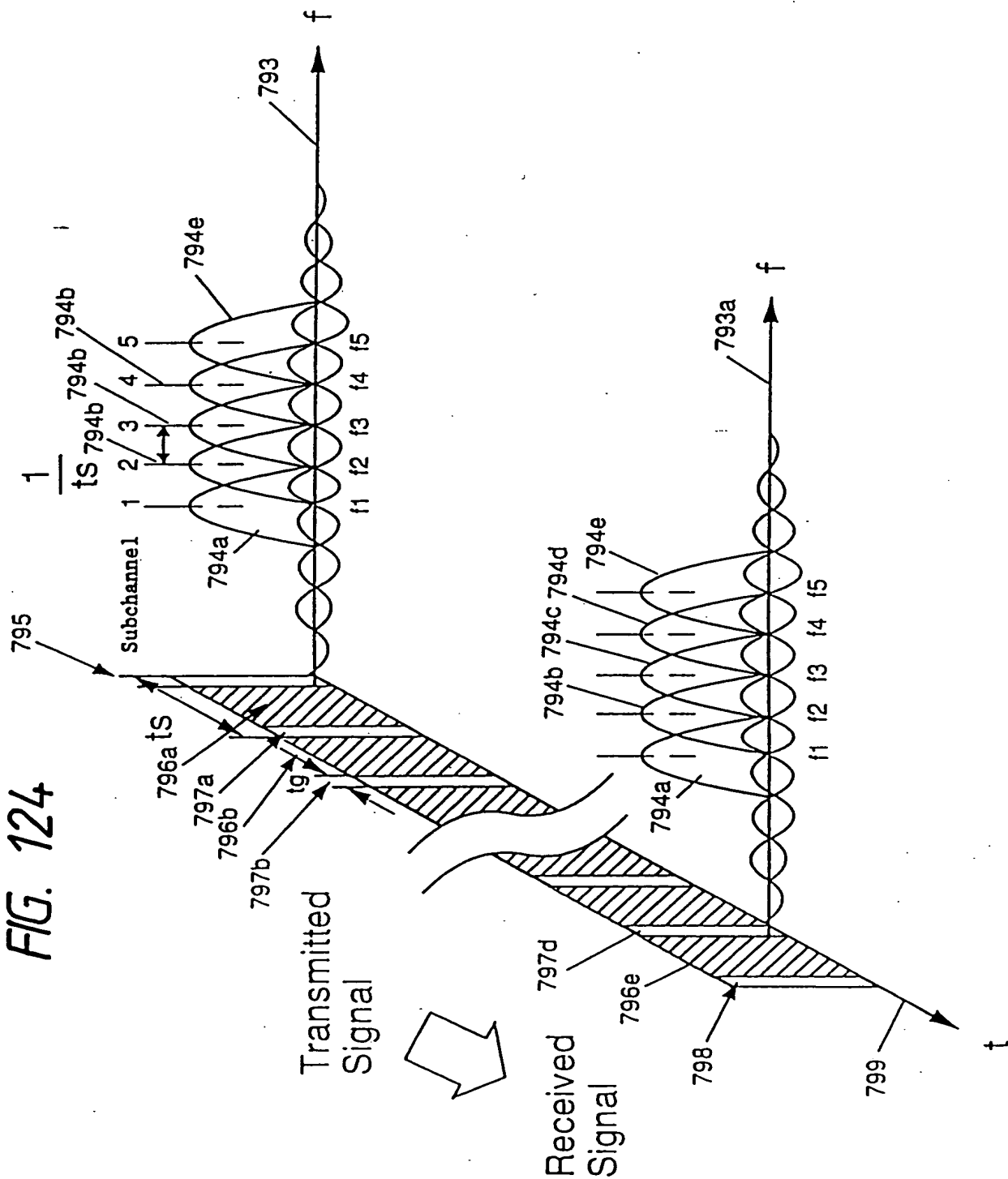
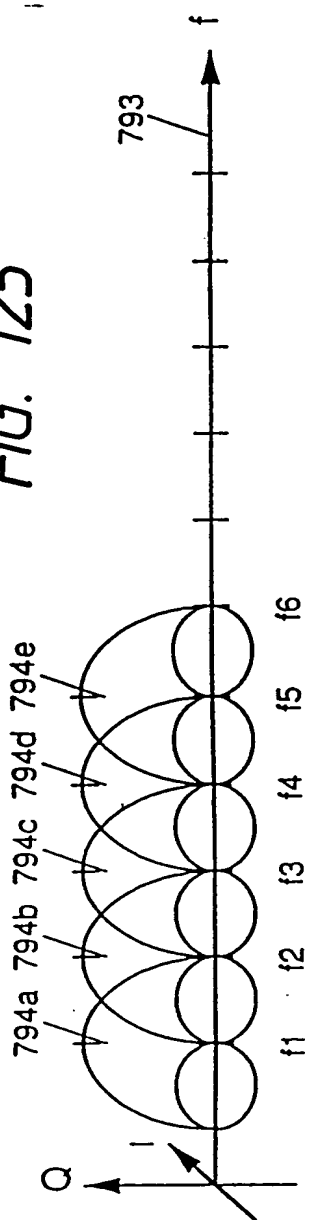
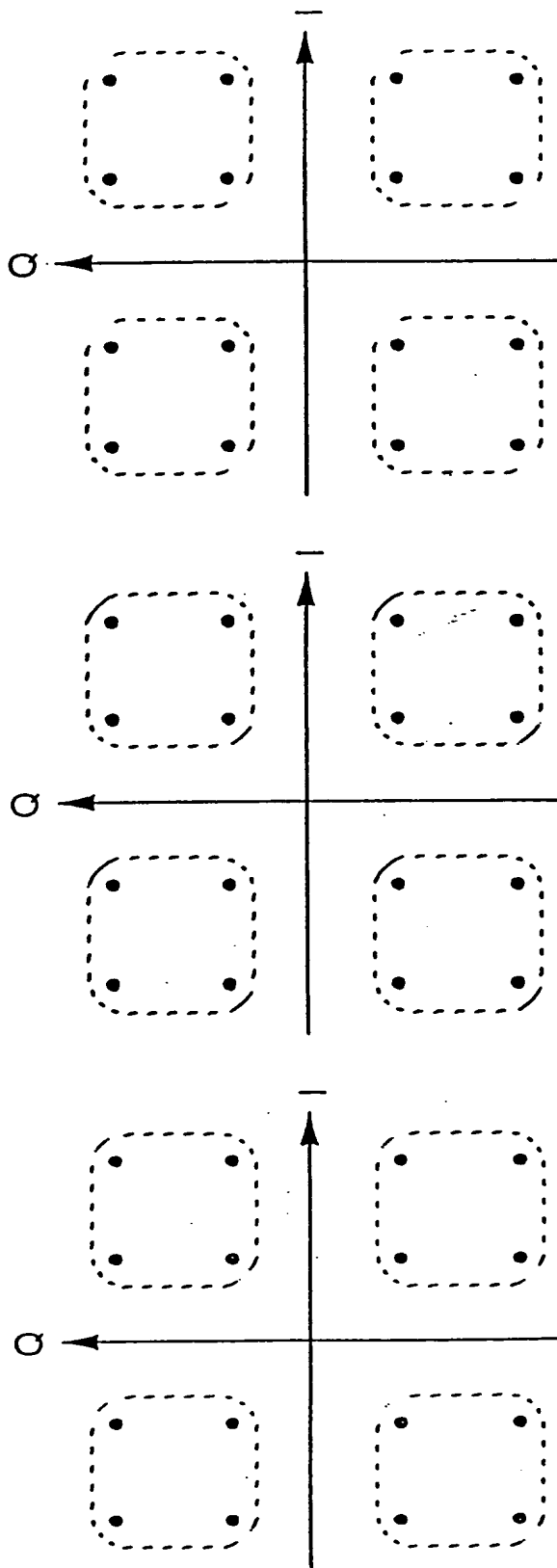


FIG. 125



(a)



(b)

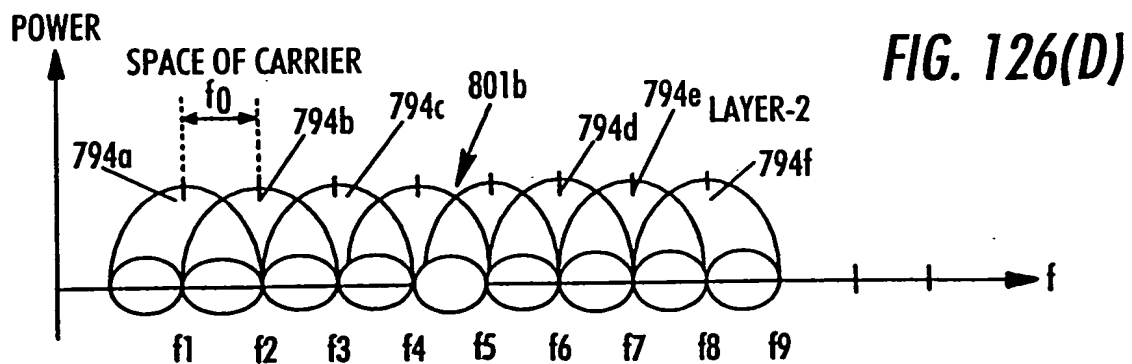
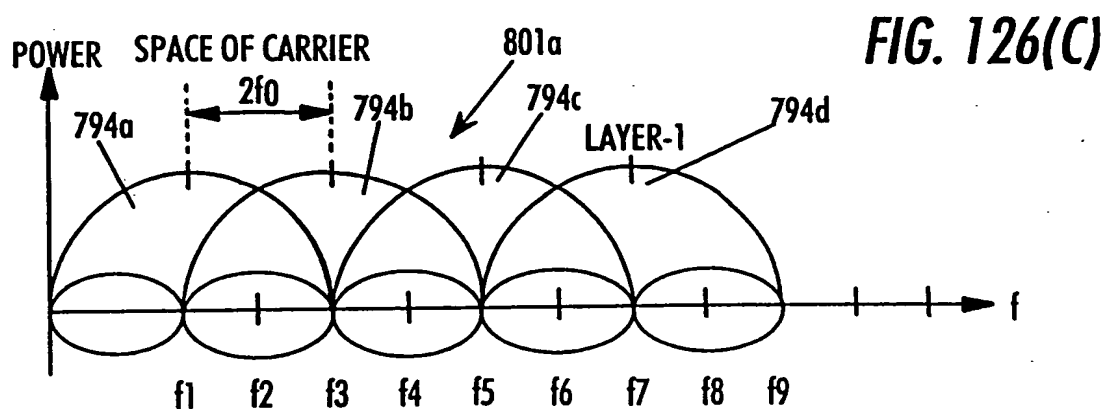
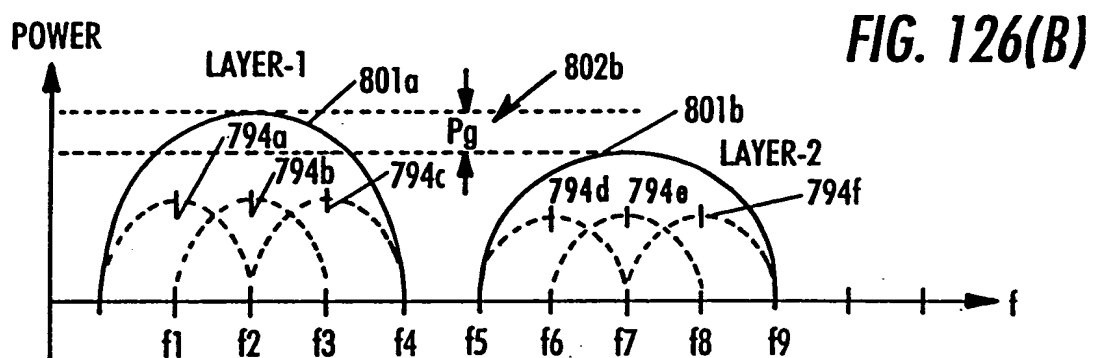
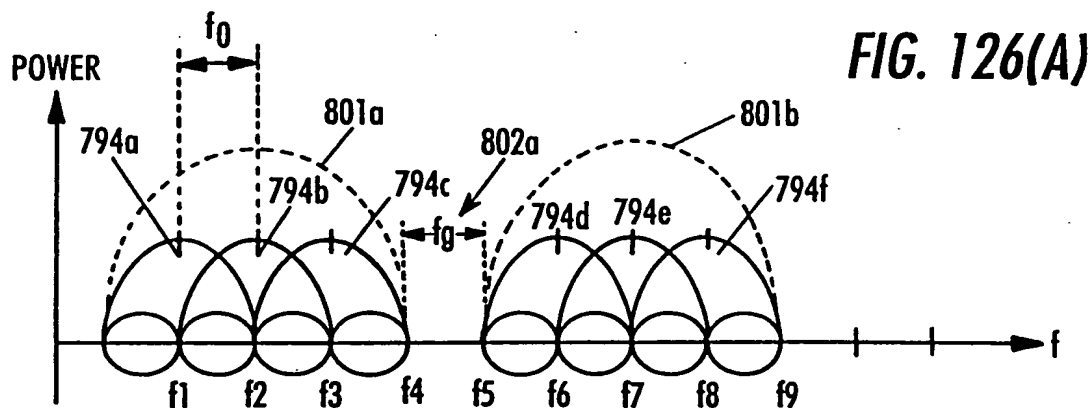
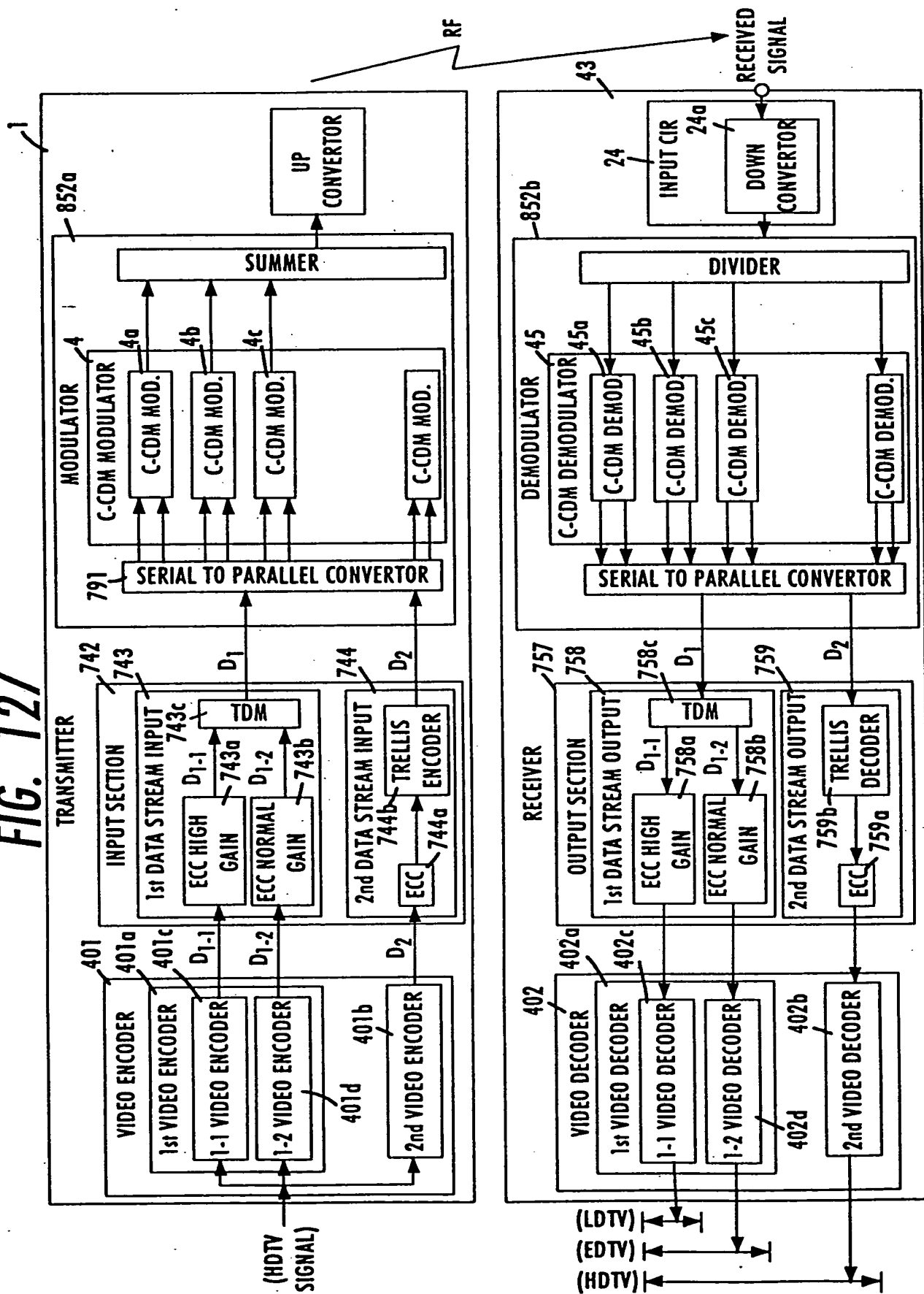


FIG. 127



744b

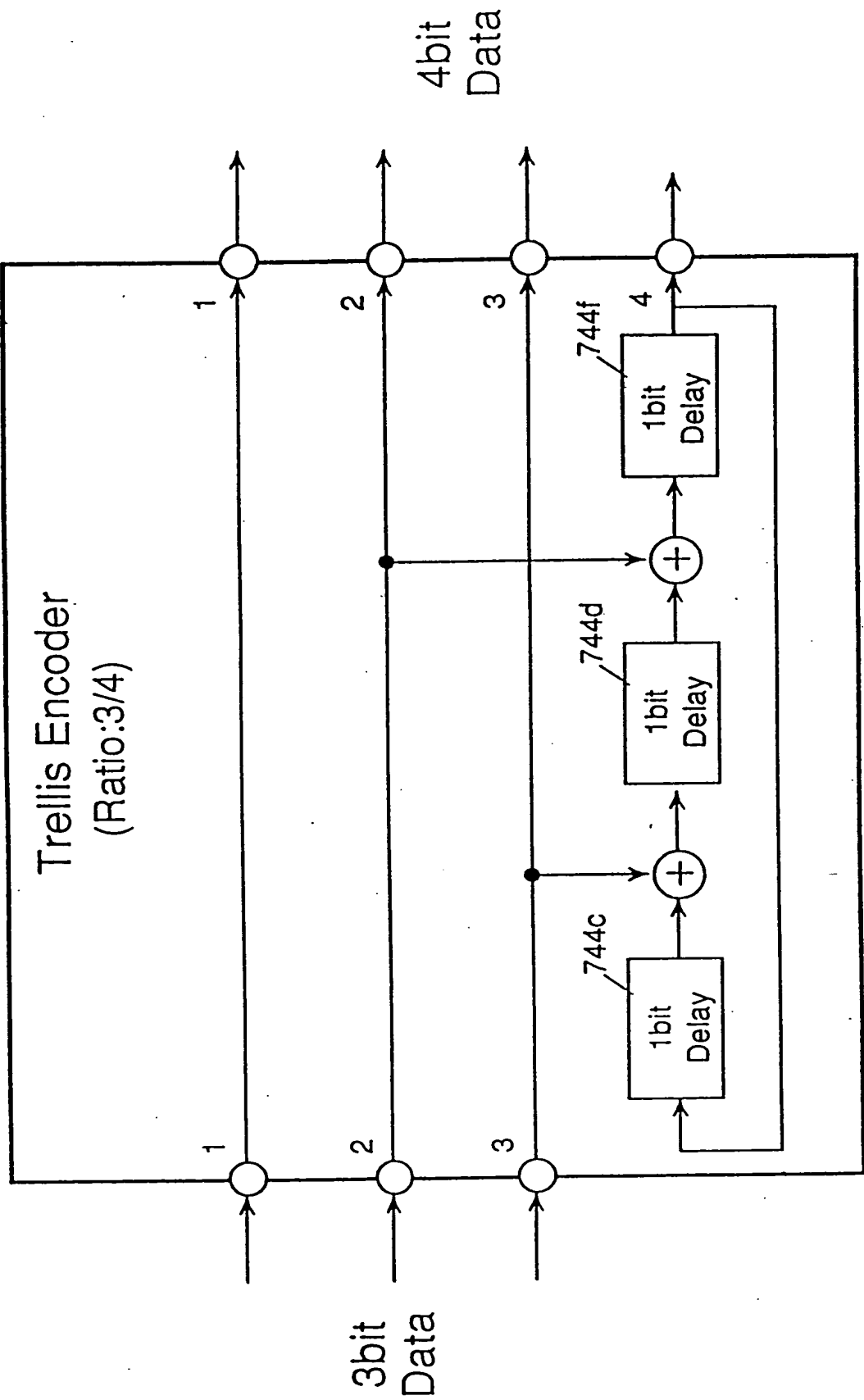




FIG. 129

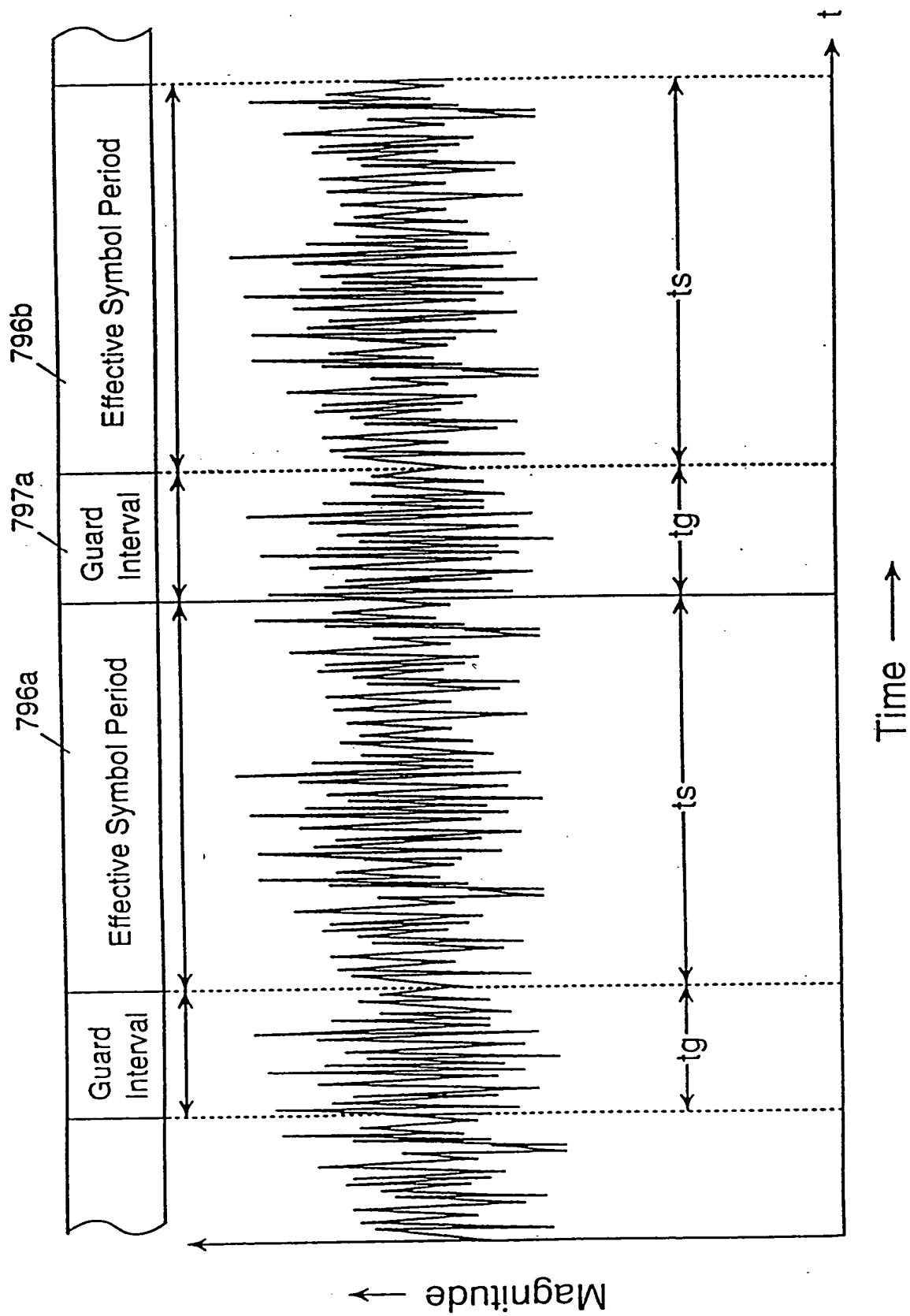
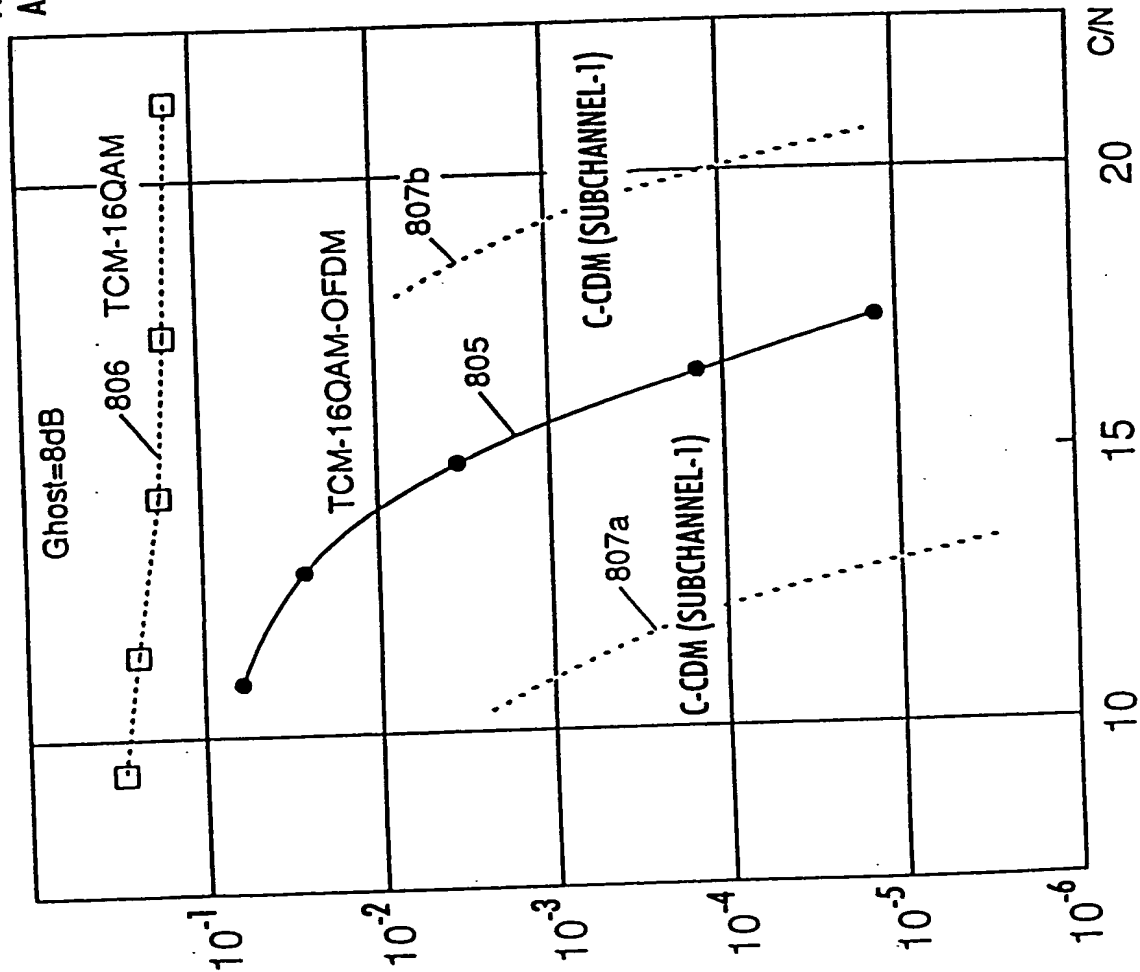


FIG. 130

GHOST DELAY = 2 $\mu$ s. D/U = 8dB  
 FIGURE 8 BIT ERROR RATE PERFORMANCE UNDER SINGLE GHOST  
 AND GAUSSIAN NOISE (1)



# FIG. 131

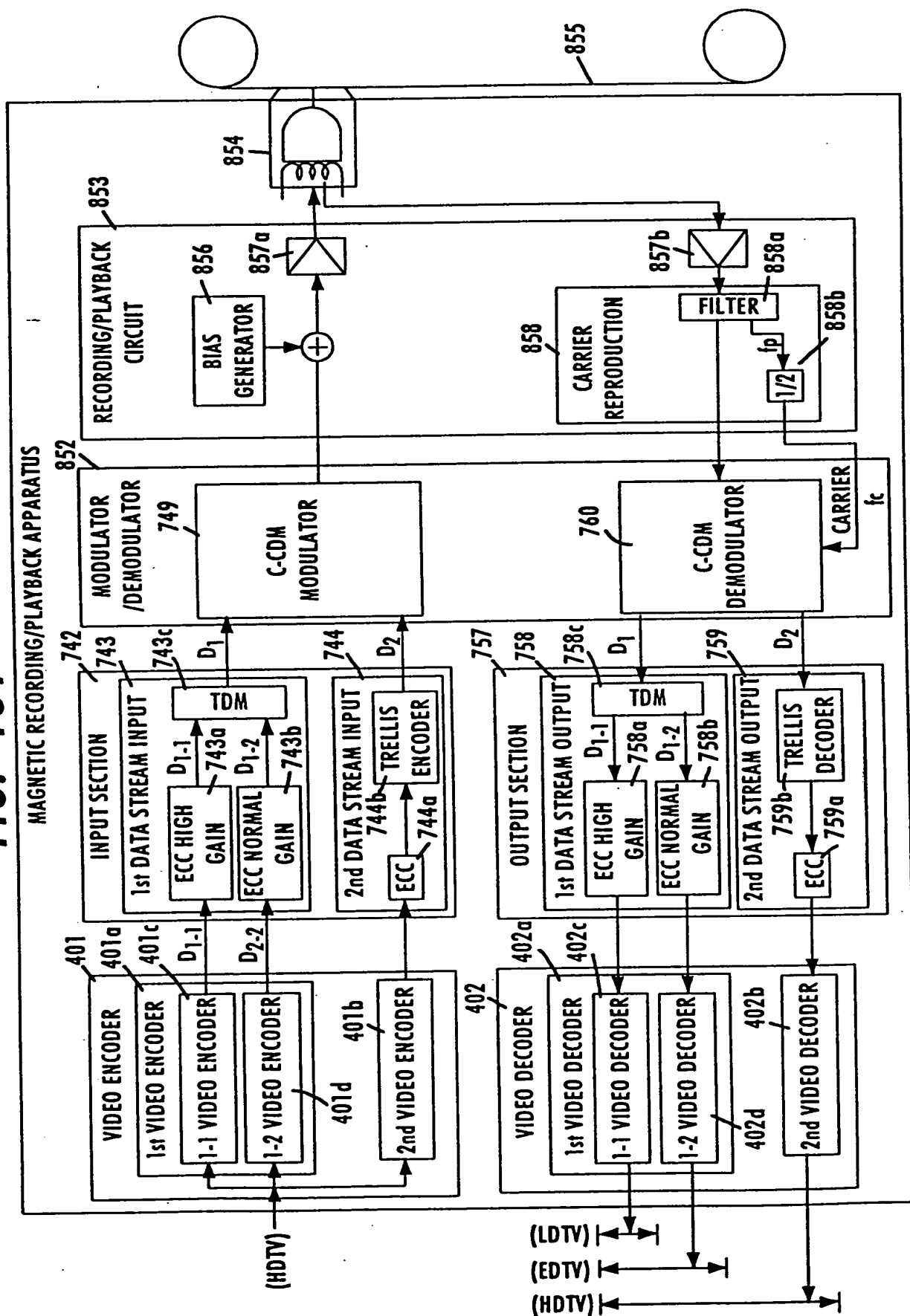


FIG. 132

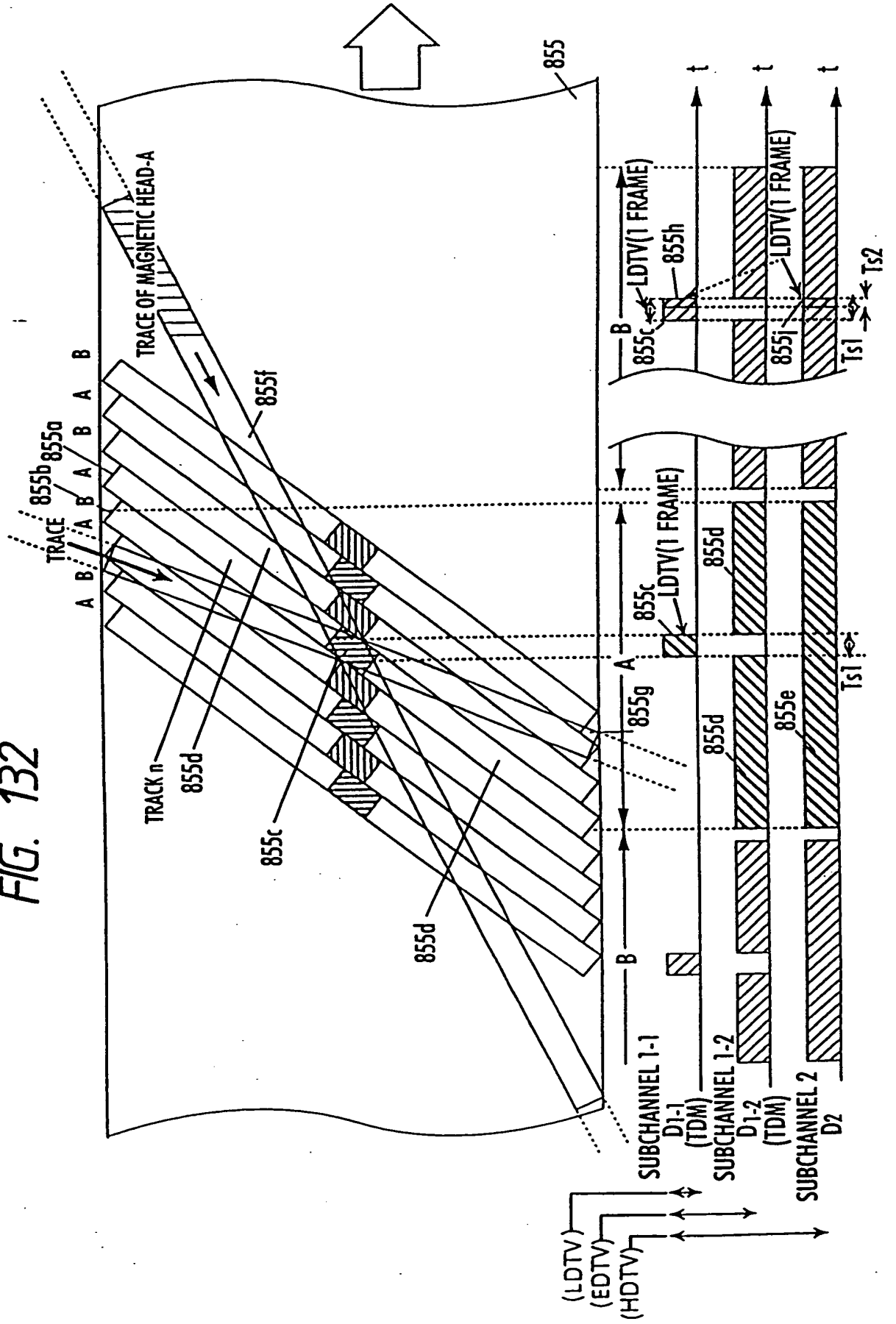


FIG. 133

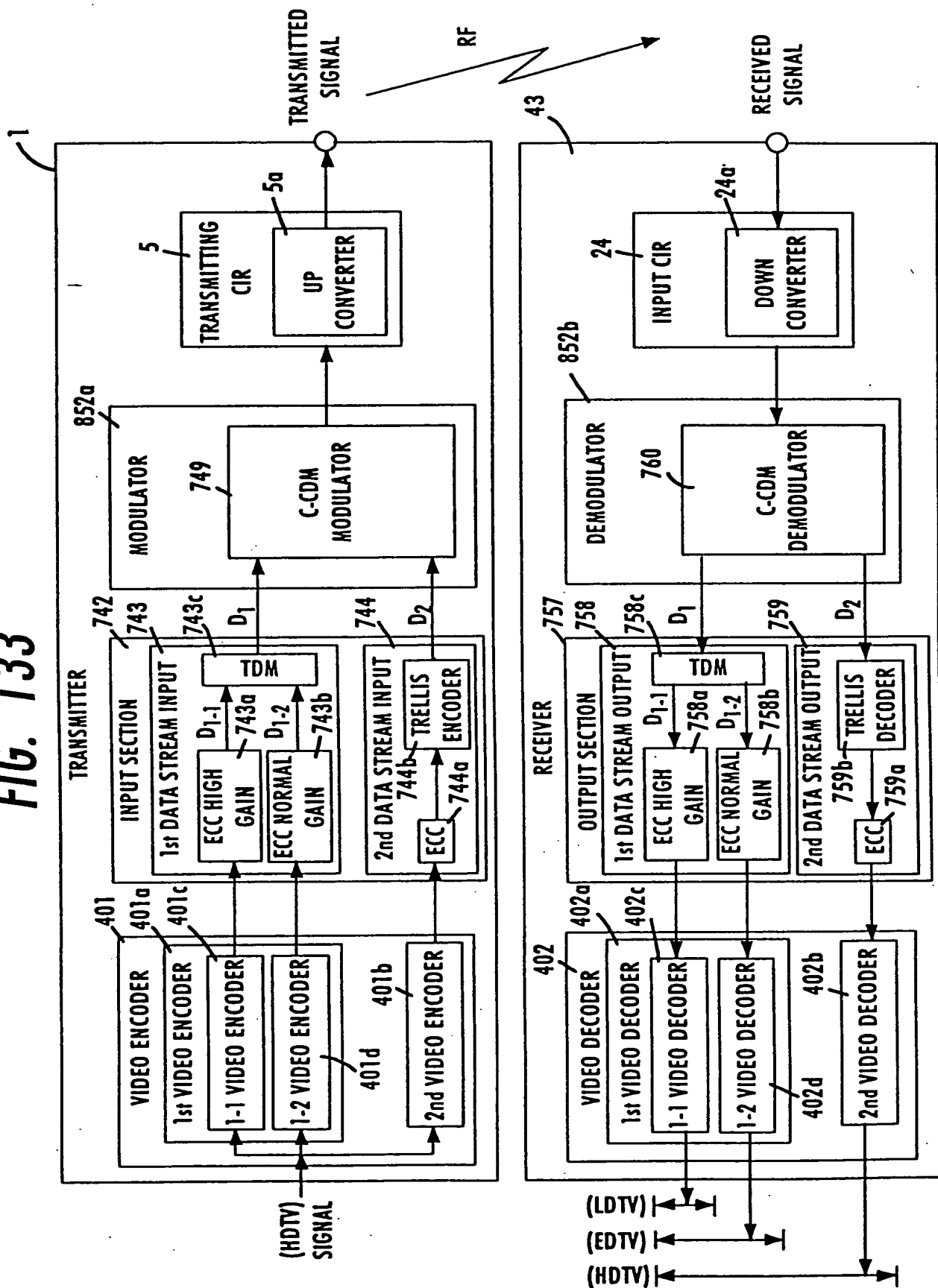


FIG. 134

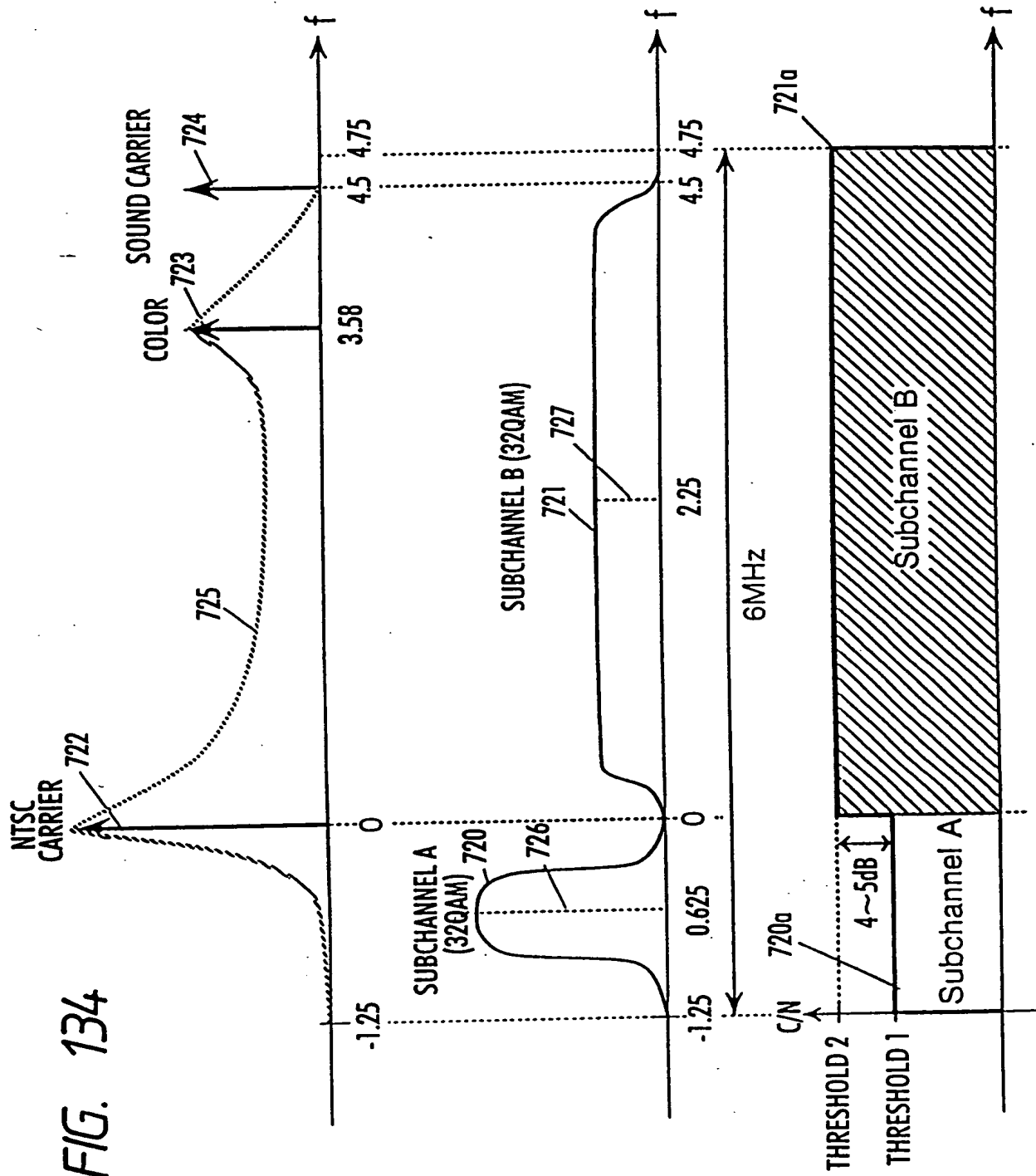


FIG. 135

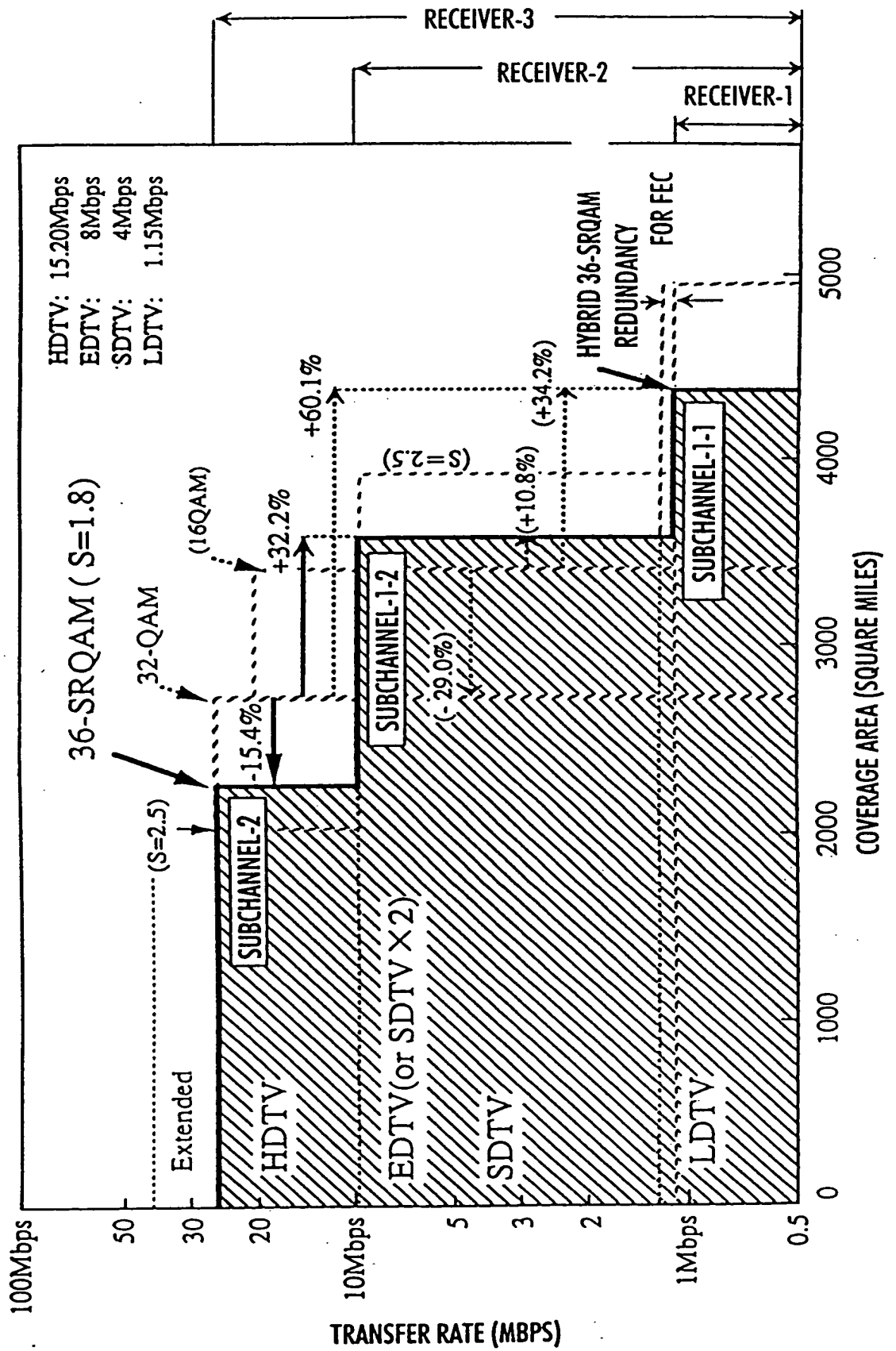


FIG. 136

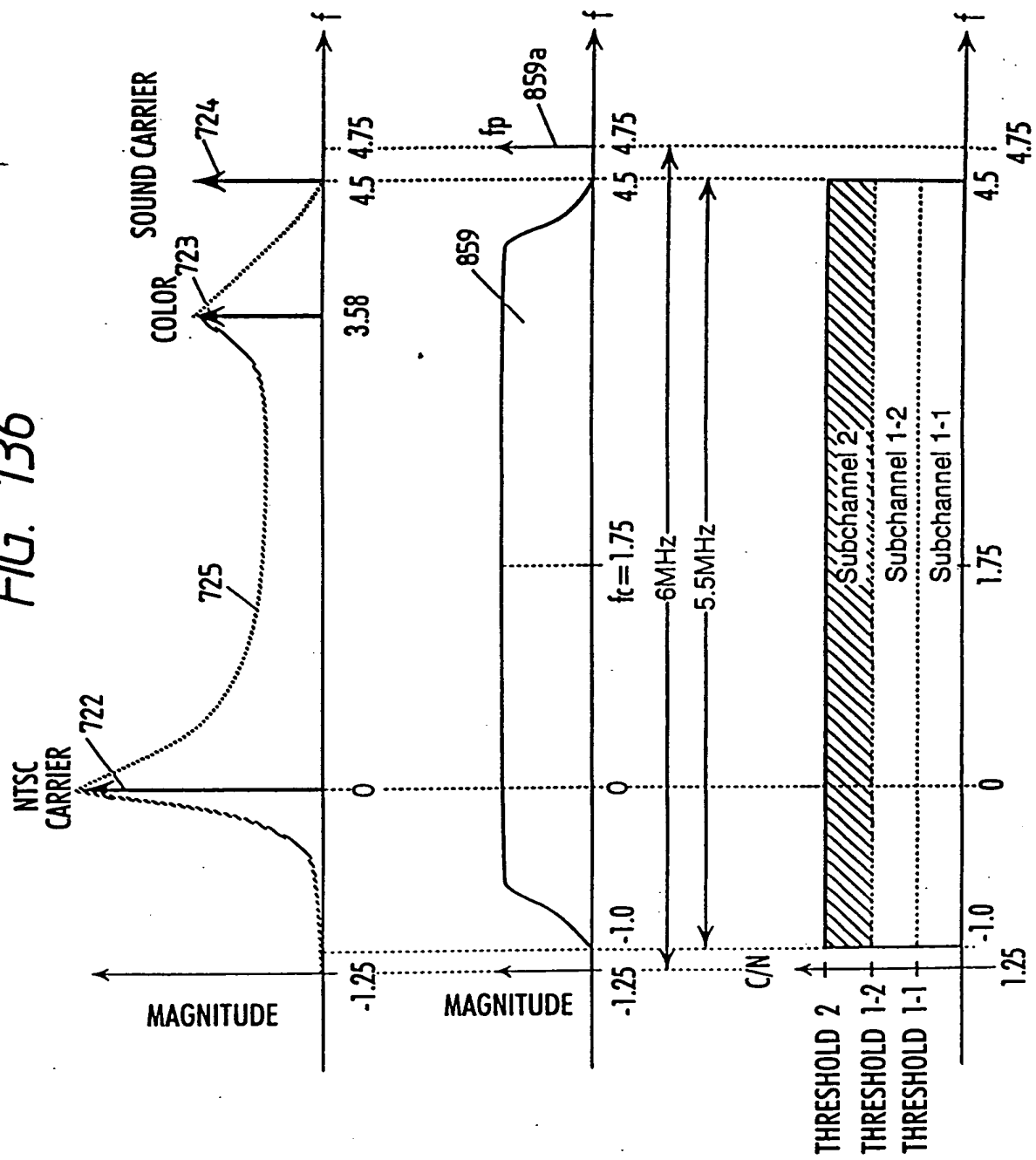




FIG. 137

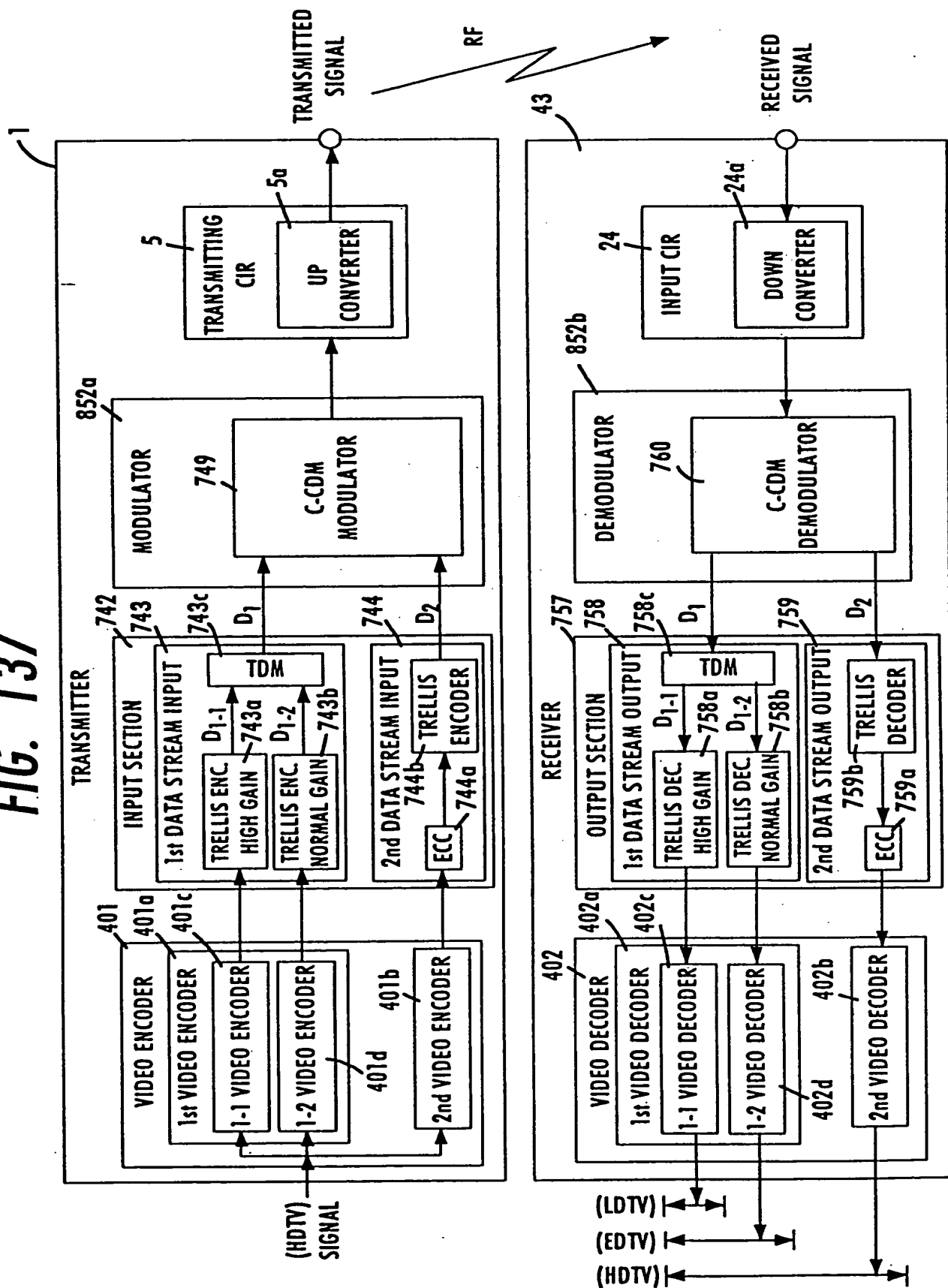


FIG. 138

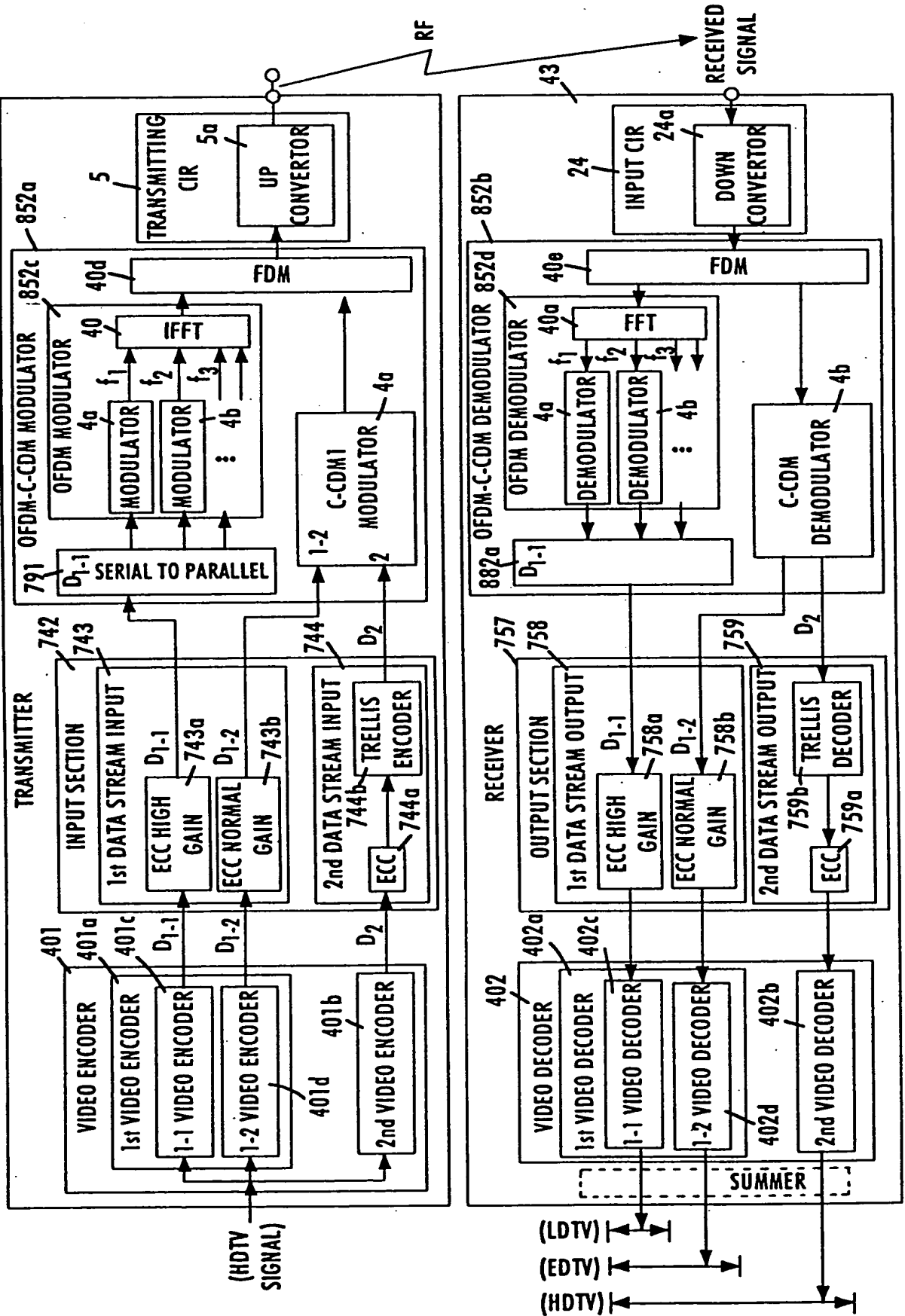
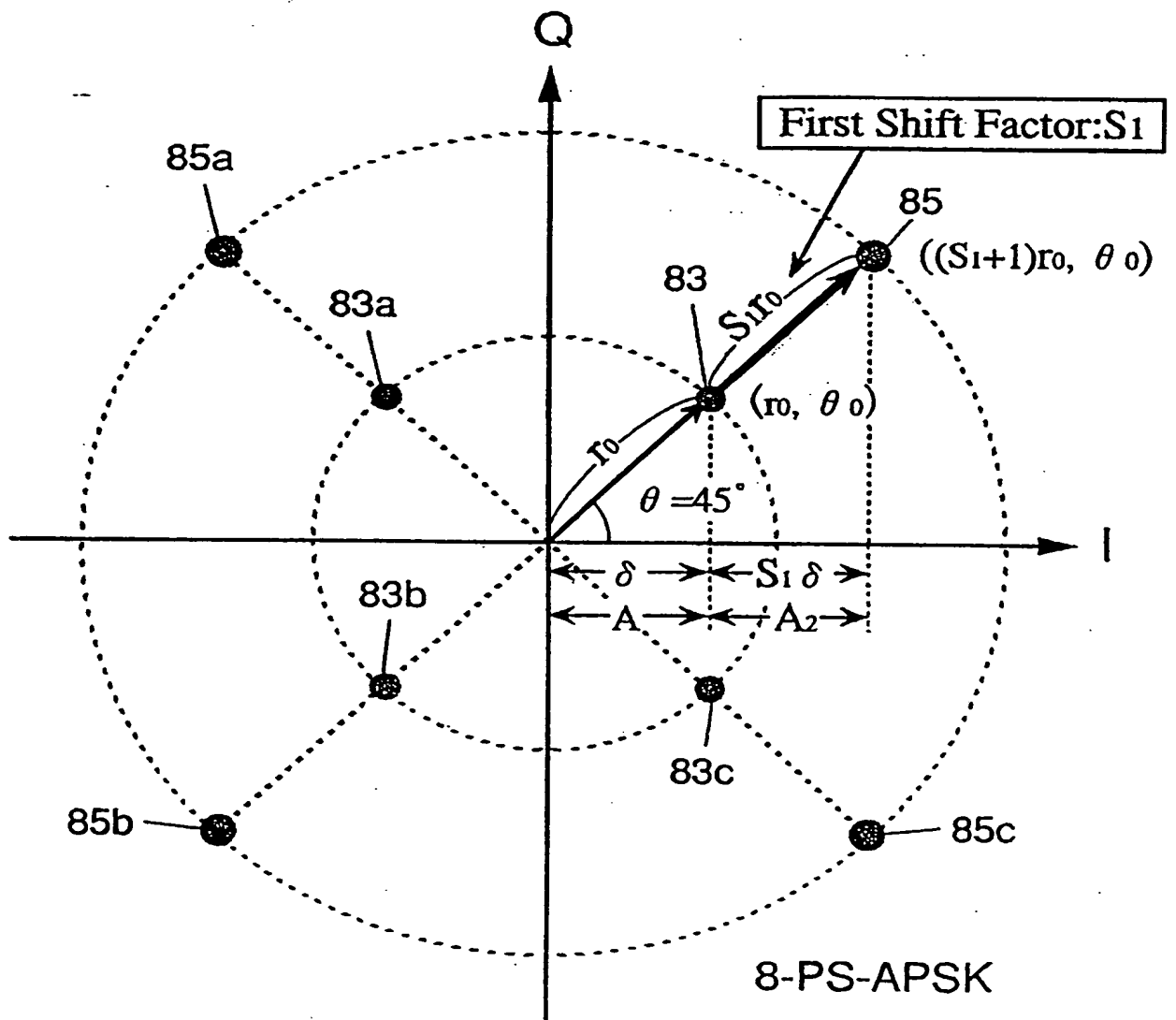


FIG. 139



**FIG. 140**

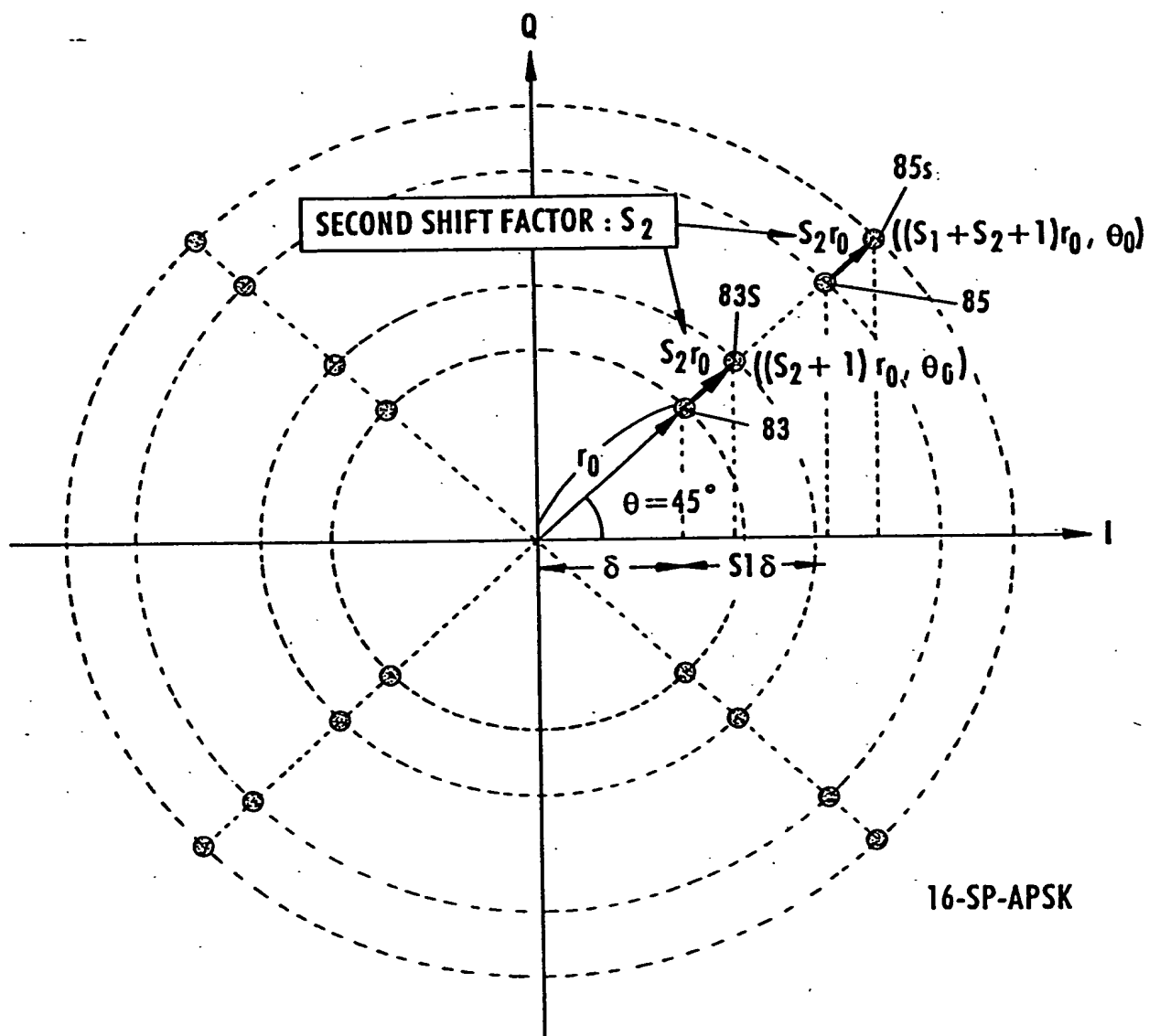


FIG. 141

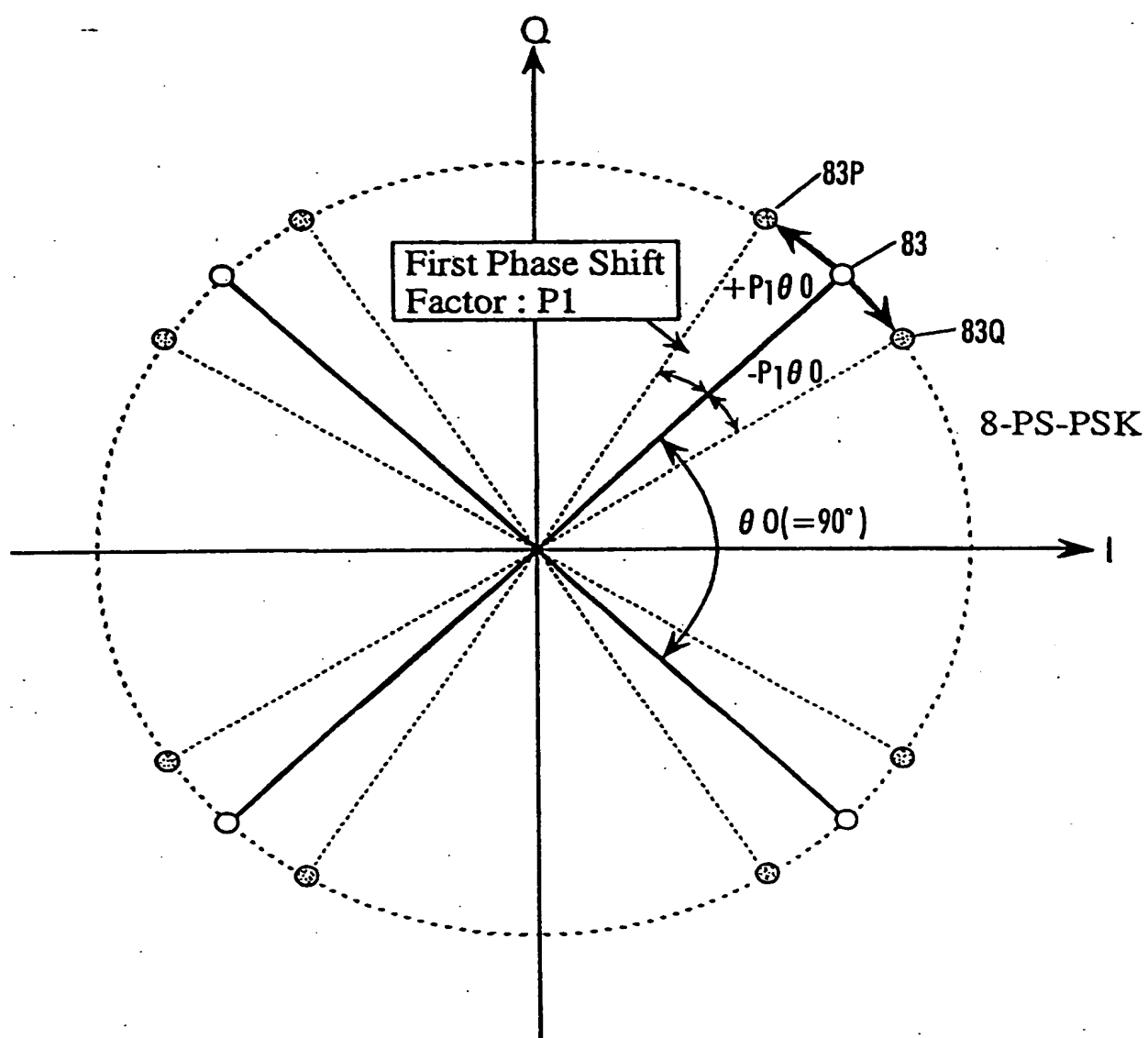


FIG. 142

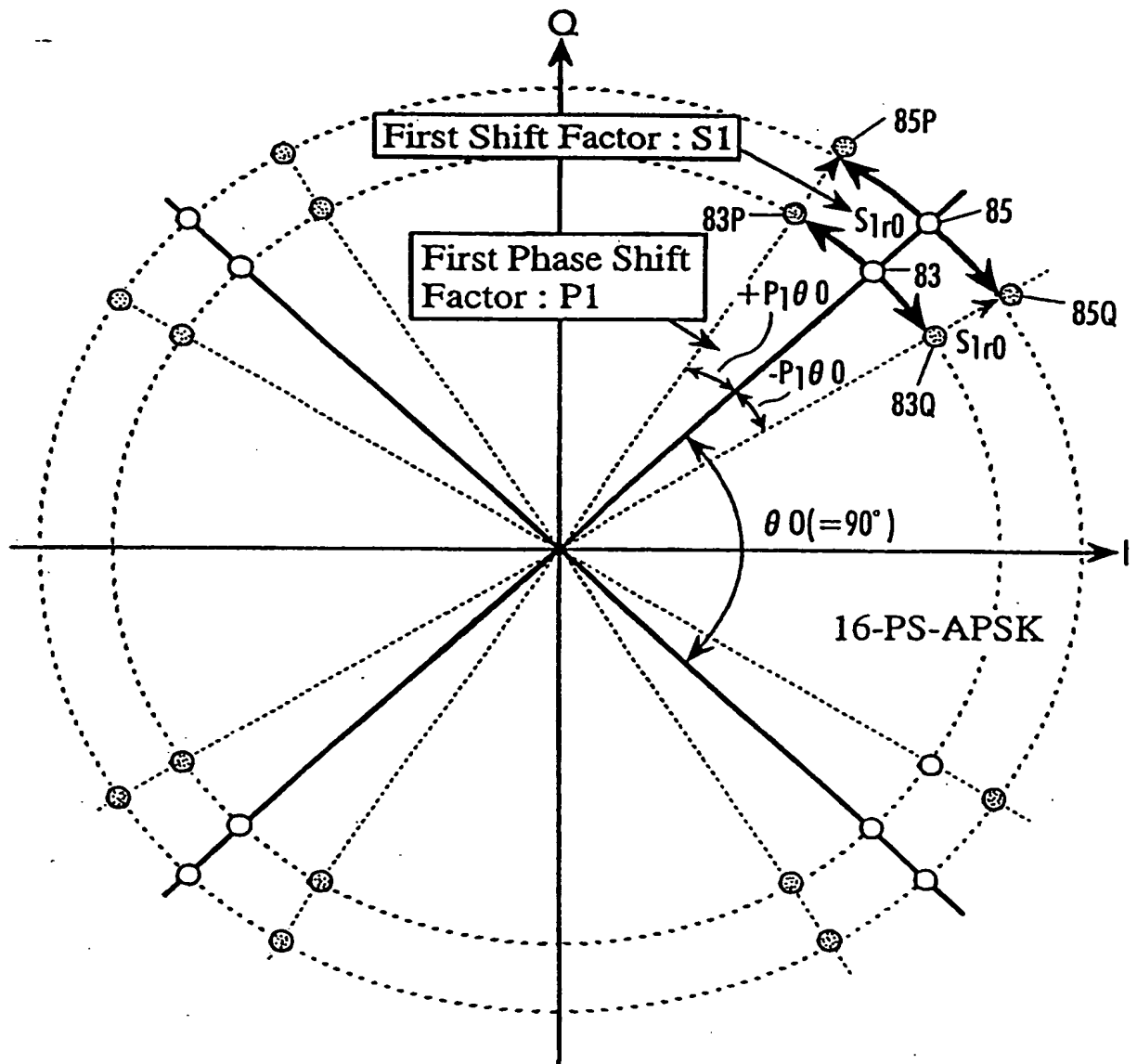
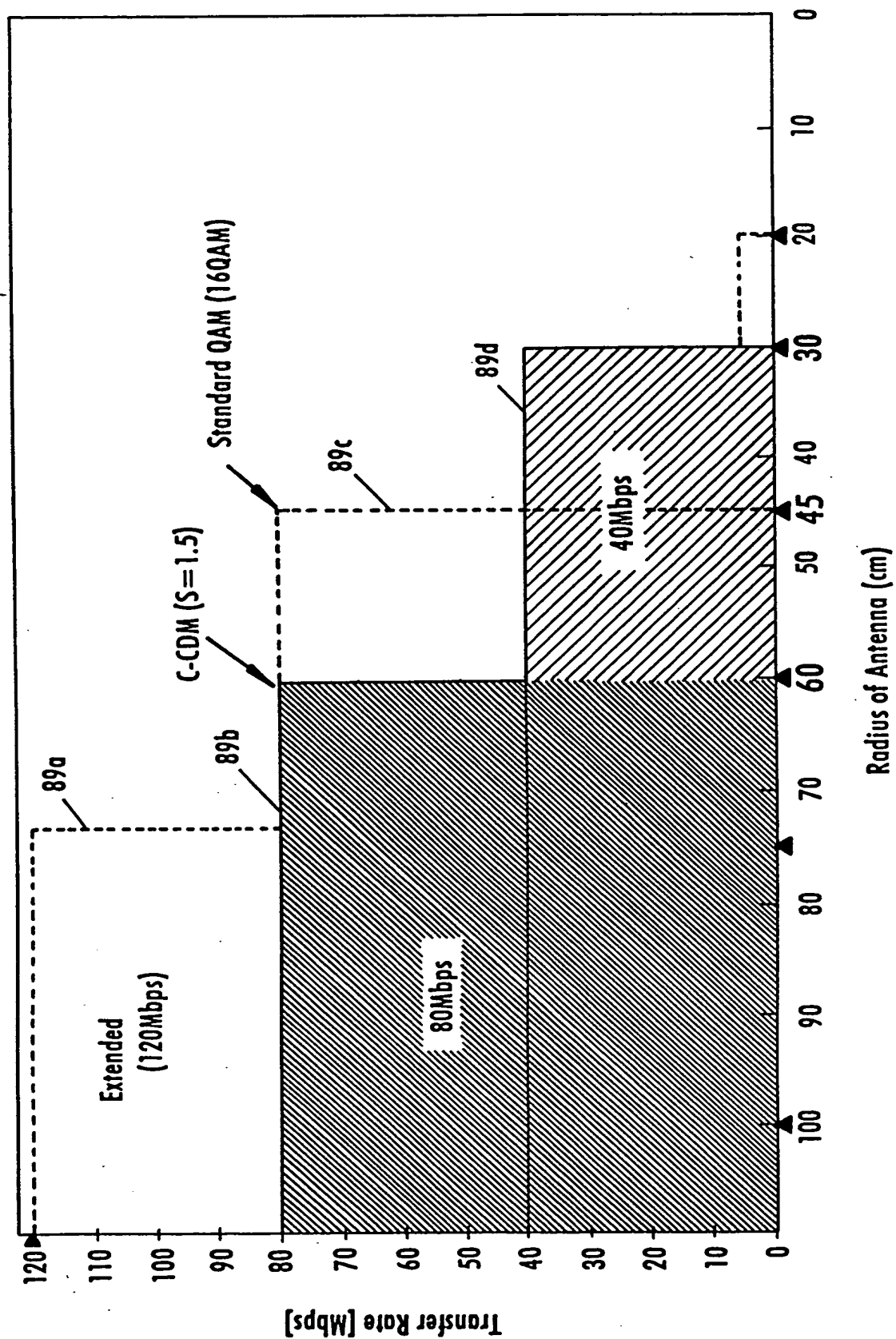


FIG. 143



**FIG. 144**

**TRANSMITTER**

The transmitter system (left) is divided into an **INPUT SECTION** (742) and a **WEIGHTED OFDM-MODULATOR** (852a).  
 In the **INPUT SECTION**, an **(HDTV SIGNAL)** is processed by a **VIDEO ENCODER** (401) consisting of a **1st VIDEO ENCODER** (401a) and a **2nd VIDEO ENCODER** (401b). The 1st video encoder outputs **D1-1** and **D1-2** signals. **D1-1** passes through an **ECC HIGH GAIN** (743a) and an **ECC NORMAL GAIN** (743b) before entering a **TDM** (743c). **D1-2** also enters the **TDM**. The **TDM** output **D1** is then processed by a **TRELLIS ENCODER** (744b) along with a **2nd DATA STREAM INPUT** (744a) to produce **D2**.  
 The **WEIGHTED OFDM-MODULATOR** (852a) takes **D1** and **D2** as inputs. It includes a **SERIAL TO PARALLEL** converter (791) and a **WEIGHTED MODULATOR** (791d) which consists of six parallel **MOD.** blocks. The outputs of these modulators are summed and then processed by an **IFFT** (40) and a **D/A CONVERTOR** (4e) to produce the **TRANSMITTING CIR** (5a), which is transmitted as an **RF** signal.

**RECEIVER**

The receiver system (right) is divided into a **WEIGHTED OFDM-DEMODULATOR** (852b) and an **OUTPUT SECTION** (757).  
 The **WEIGHTED OFDM-DEMODULATOR** (852b) receives a **RECEIVED SIGNAL** through an **INPUT CIR** (24a) and a **DOWN CONVERTOR** (24). The signal is then processed by an **A/D CONVERTOR** (40c) and an **FFT** (40a). The output is fed into a **WEIGHTED DEMODULATOR** (45a) which consists of six parallel **DEMOD.** blocks. The outputs of these demodulators are summed and then processed by a **SERIAL TO PARALLEL** converter (791b) to produce **D1** and **D2**.  
 The **OUTPUT SECTION** (757) takes **D1** and **D2** as inputs. **D1** passes through an **ECC HIGH GAIN** (758a) and an **ECC NORMAL GAIN** (758b) before entering a **TDM** (758c). **D2** also enters the **TDM**. The **TDM** output **D1-1** is then processed by a **TRELLIS DECODER** (759b) along with a **2nd DATA STREAM OUTPUT** (759a) to produce **D2**.  
 The **OUTPUT SECTION** also includes a **VIDEO DECODER** (402) consisting of a **1st VIDEO DECODER** (402a) and a **2nd VIDEO DECODER** (402b). The 1st video decoder outputs **D1-1** and **D1-2** signals. **D1-1** passes through an **ECC HIGH GAIN** (758a) and an **ECC NORMAL GAIN** (758b) before entering a **TDM** (758c). **D1-2** also enters the **TDM**. The **TDM** output **D1** is then processed by a **TRELLIS DECODER** (759b) along with a **2nd DATA STREAM OUTPUT** (759a) to produce **D2**.  
 The **OUTPUT SECTION** also includes a **SUMMER** (402d) which combines the outputs of the video decoders to produce the final **(LDTV)**, **(EDTV)**, and **(HDTV)** signals.

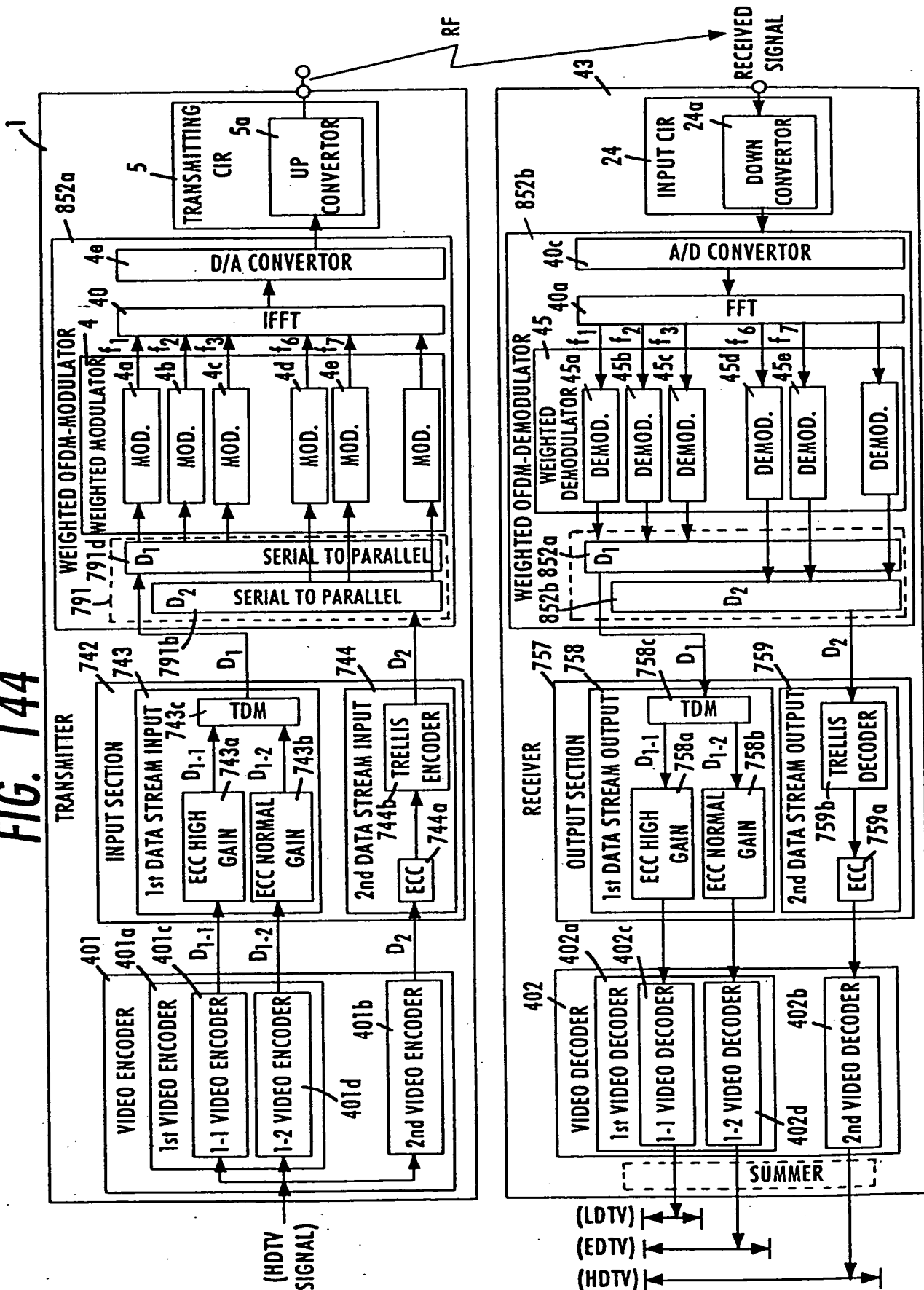




FIG. 145(A)

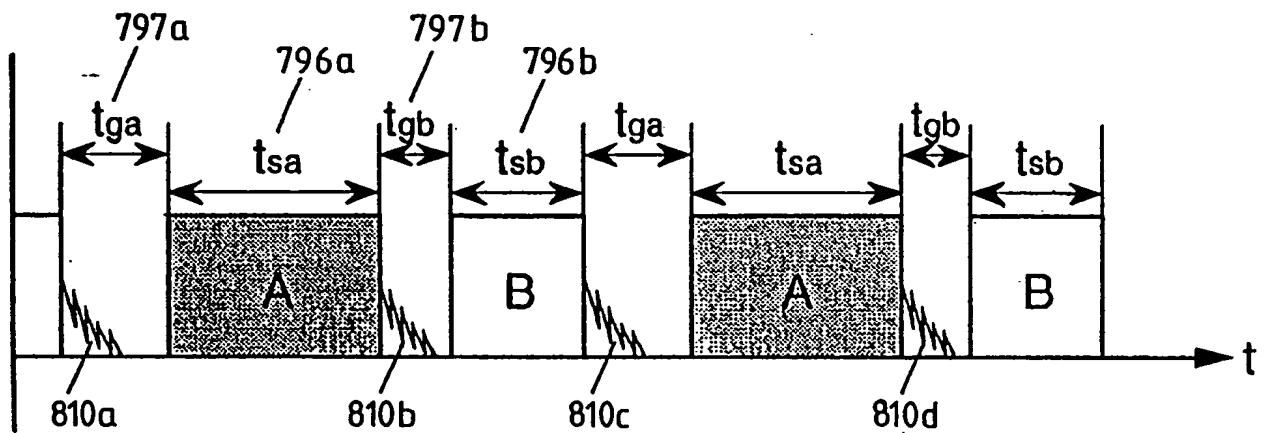


FIG. 145(B)

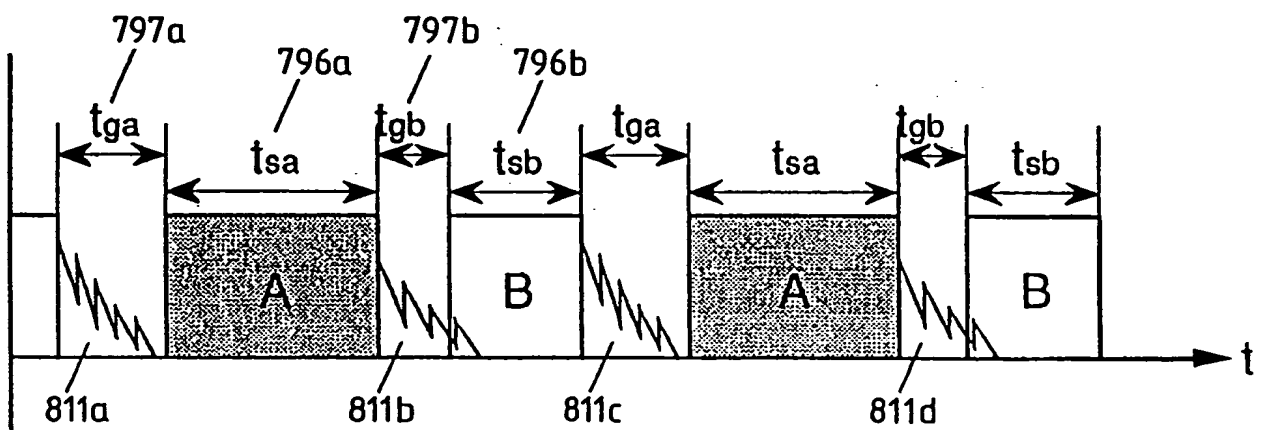
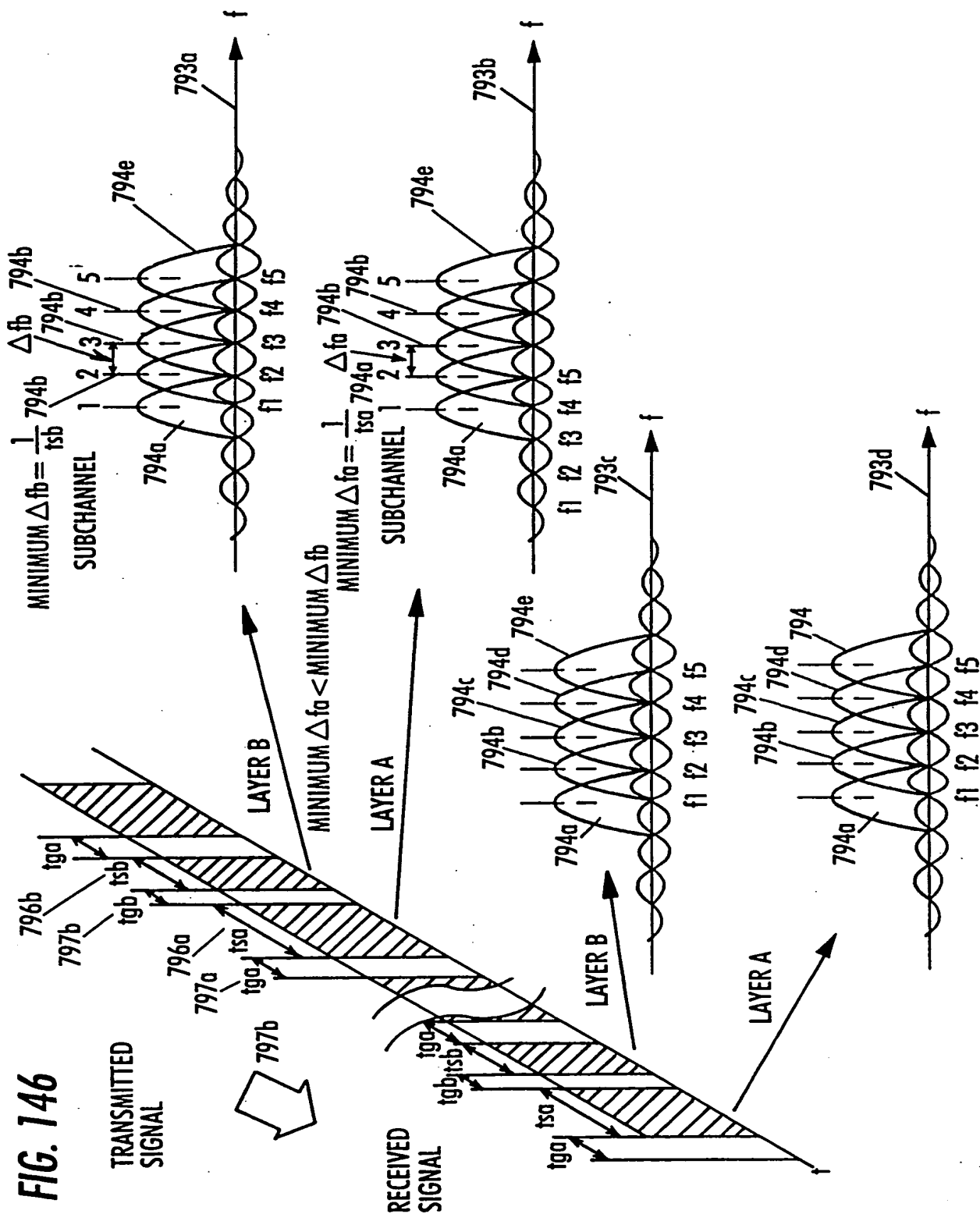


FIG. 146



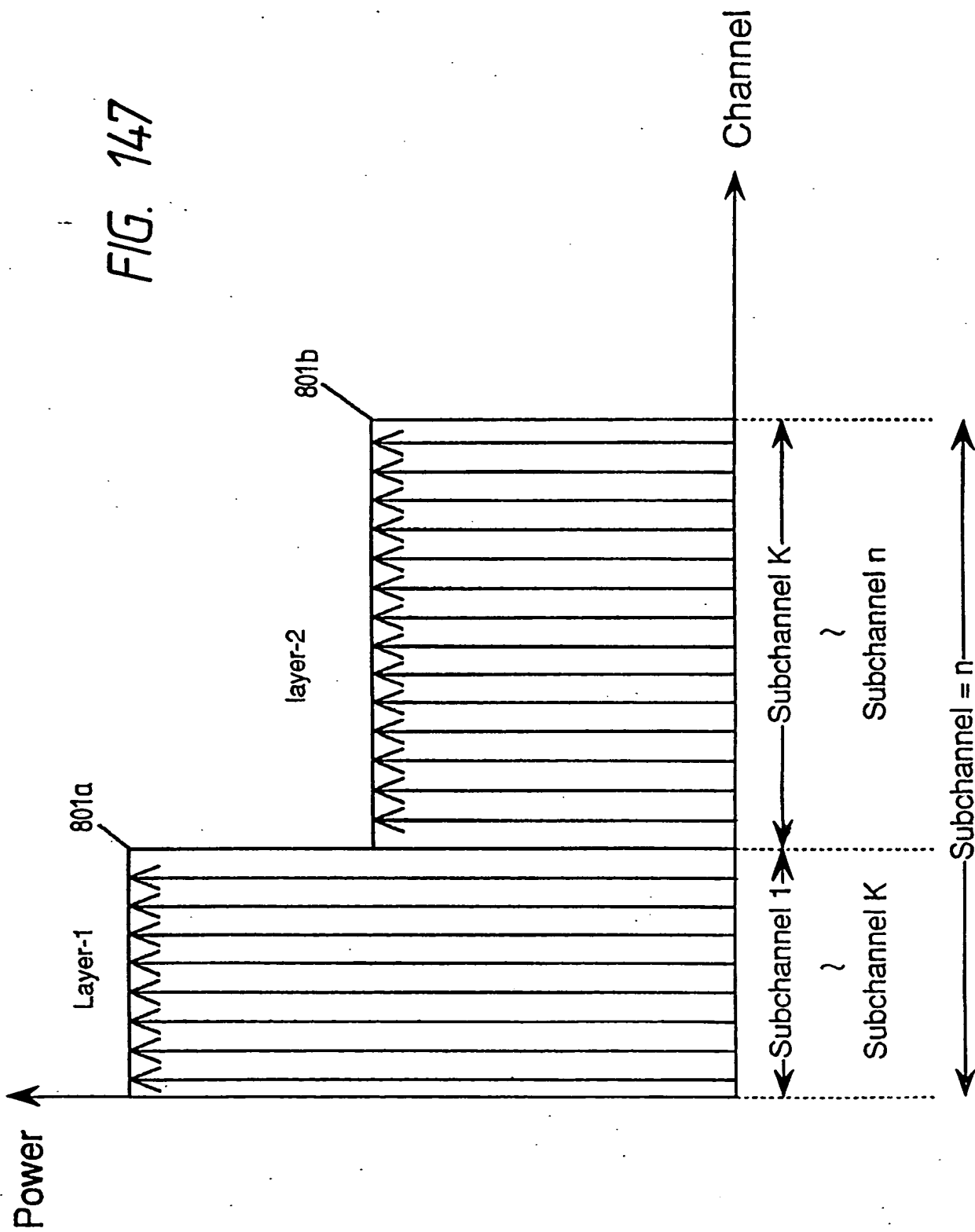
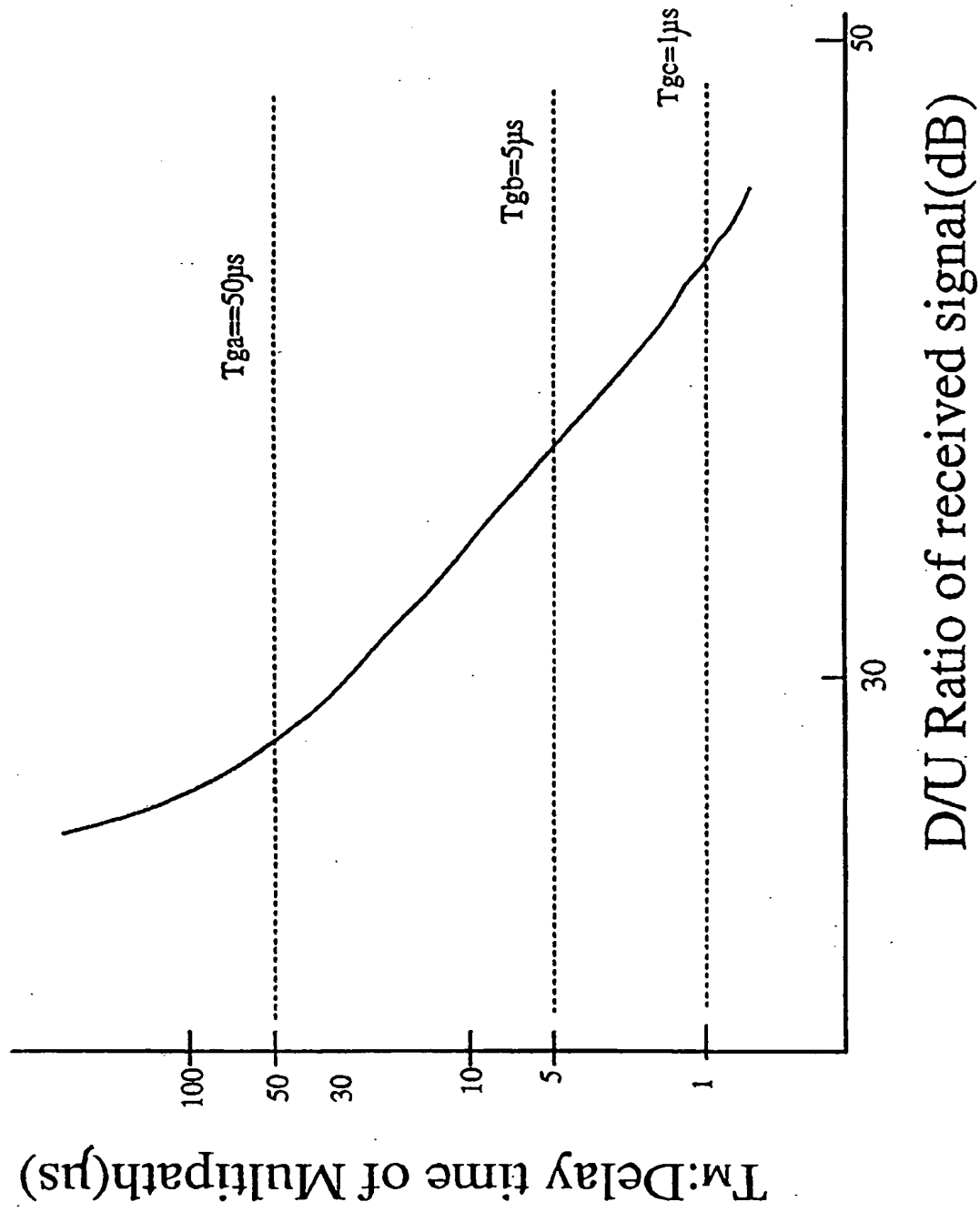


FIG. 147

FIG. 148



The diagram illustrates the timing relationship between three layers of OFDM signals, labeled LAYER-1, LAYER-2, and LAYER-3. The vertical axis represents time, with a time scale  $t$  indicated at the top.

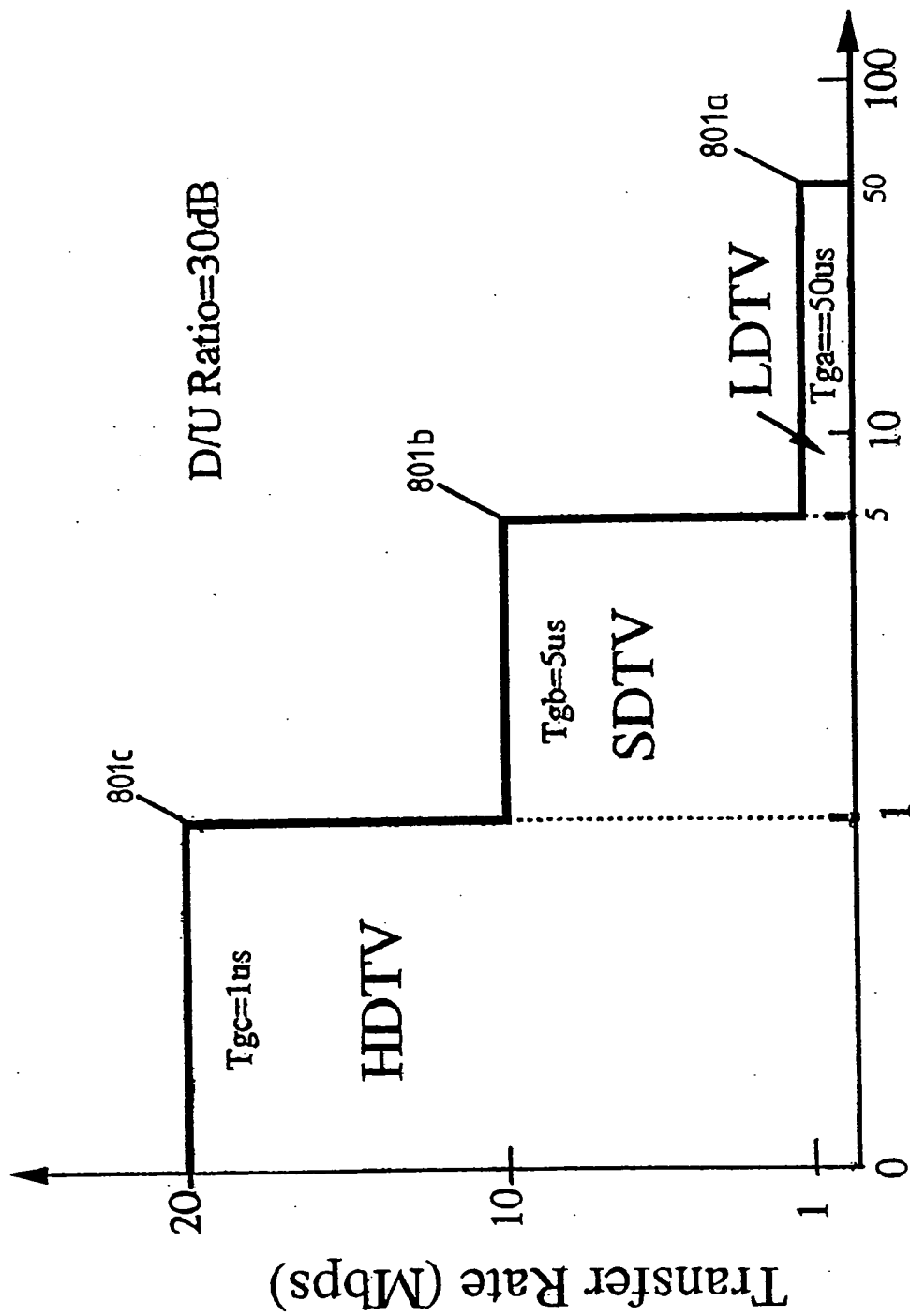
**LAYER-1:** Shows a signal with a guard interval  $T_{ga}$  and a carrier spacing of  $200\mu s$ . The signal is labeled  $797a$  and  $796a$ . A shaded region indicates the guard interval.

**LAYER-2:** Shows a signal with a guard interval  $T_{gb}$  and a carrier spacing of  $150\mu s$ . The signal is labeled  $797b$  and  $796b$ . A shaded region indicates the guard interval.

**LAYER-3:** Shows a signal with a guard interval  $T_{gc}$  and a carrier spacing of  $100\mu s$ . The signal is labeled  $797c$  and  $796c$ . A shaded region indicates the guard interval.

The diagram also shows the relationship between the guard interval and the carrier spacing, with a  $50\mu s$  interval between the start of the guard interval and the start of the carrier spacing. The diagram is labeled **GUARD INTERVAL TIME WEIGHTED-OFDM** and **CARRIER SPACING WEIGHTED-OFDM**.

FIG. 150



$T_M$ : Delay time of Multipath(us)

FIG. 151

